Gate-emitter Pre-threshold Voltage as a Health Sensitive Parameter for IGBT Chip Failure Monitoring in High Voltage Multichip IGBT Power Modules

Richard Mandeya¹, Cuili Chen¹, Volker Pickert¹, *Member, IEEE*, R.T. Naayagi², *Senior Member, IEEE*, Bing Ji³, *Senior Member, IEEE*.

¹School of Engineering, Newcastle University, NE1 7RU, Newcastle upon Tyne, UK, England.

²School of Electrical and Electronic Engineering, Newcastle University International Singapore, 567739, Singapore.

³Department of Engineering, University of Leicester, LE1 7RH, Leicester, UK, England.

m.a.r.mandeya@ncl.ac.uk, c.chen22@ncl.ac.uk, volker.pickert@ncl.ac.uk, naayagi.ramasamy@ncl.ac.uk, bing.ji@le.ac.uk.

Abstract— This paper proposes a novel health sensitive parameter, called the gate-emitter pre-threshold voltage $V_{GE(pre-th)}$, for detecting IGBT chip failures in multichip IGBT power modules. The proposed method has been applied in an IGBT gate driver and measures the V_{GE} at a fixed time instant of the V_{GE} transient before the threshold voltage occurs. To validate the proposed method, theoretical analysis and practical results for a 16-chip IGBT power module are presented in the paper. The results show a 500 mV average shift in the measured $V_{GE(pre-th)}$ for each IGBT chip failure.

Index Terms— High voltage multichip Insulated Gate Bipolar Transistor (IGBT) module, IGBT chip failure, health monitoring, threshold voltage.

I. INTRODUCTION

IGBT power modules are widely used in high power converter applications [1, 2]. They dominate the market due to their superior overall performance which results from their structure incorporating the gating of Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) for fast switching speed, and the body region of Bipolar Junction Transistors (BJTs) for low conduction losses [3, 4]. Recently, there has been a growing interest in the application of health monitoring techniques to improve the operational reliability of the IGBT power modules. In general, there are mainly three points which are of interest in IGBT health monitoring: i) virtual junction temperature (T_v) [5-28], ii) solder degradation [29-32], and iii) bond wire failure [29, 33-39]. Some of the health monitoring techniques proposed are in-situ, meaning health monitoring is achieved via a test circuit exclusively developed for detecting degradation and implemented onboard power converters. In-situ health monitoring avoids the fallout of a disrupted field service due to power converter teardown prior to inspection.

This paper proposes an online detection technique for IGBT chip failures in High Voltage (HV) multichip IGBT power modules as their applications are mostly critical [40-42]. A typical multichip module is depicted in Fig.1 which shows a 3.3 kV, 800 A single switch IGBT power module (DIM800NSM33-F) from Dynex Semiconductor Limited that was used for experimentation. The DIM800NSM33-F has 16 IGBT chips and 8 anti-parallel diodes. This work focusses only on the health monitoring of the IGBT chips and not the diode chips. This is because IGBTs have a more complex

semiconductor structure and due to the gate a more complex chip surface structure which makes IGBT chip less reliable compared to diodes. Also, IGBTs experience higher turn-on and turn-off losses compared to diodes and are therefore more stressed. Finally, in large power modules, it is common to have more IGBT chips than diode chips due to the different current density for each device type.

Fig. 1. Dynex 3.3 kV, 800 A IGBT Power Module (DIM800NSM33-F): Electrical Configuration [43], External and Interior View.

Bond wire failure is one of the primary failure mechanisms of the IGBT module. For an IGBT chip, since several bond wires are employed for the chip connection, it remains functional upon the initial occurrence of one bond wire lift-off. However, an IGBT chip eventually ceases to function when all of its bond wires fail. Likewise, upon the initial chip failure, a multichip IGBT module still remains functional due to several IGBT chips being in parallel [33, 44]. Nevertheless, an IGBT power module's robustness is in line with its health conditions which depends on each of the constituent chips. Eventually, the power module fails outright. In this regard, this paper proposes the IGBT chip failure as a health monitoring precursor for multichip IGBT power modules.

A new method for detecting the IGBT chip failures in multichip HV IGBT power modules is presented in this paper by monitoring the pre-threshold voltage ($V_{GE(pre-th)}$) which takes place during the turn-on transient of gate-emitter voltage V_{GE} . A distinct advantage of leveraging $V_{GE(pre-th)}$ is that it is measured prior to the IGBT collector current (I_C) rise or the collector emitter voltage decline, and hence the integrated readout circuit is less susceptible to noise caused by the current and voltage commutations in line with the durations after the threshold point is surpassed. Furthermore, $V_{GE(pre-th)}$ does not require HV isolation and HV insulation from collector as all of the measurement circuitry is on the gate side rather than the HV collector side. For HV isolation, we refer to the electric circuitry employed for isolation between the HV and gate-emitter circuits. For HV insulation, we mean the insulation of the cables

and the components. Unlike current sensor based methods, $V_{GE(pre-th)}$ uses a simple low cost and lightweight voltage sensor which can be easily embedded into any gate driver. This paper discusses the theoretical analysis and hardware implementation of $V_{GE(pre-th)}$ on the gate driver of the 16-chip DIM800NSM33-F, where $V_{GE(pre-th)}$ is monitored at a fixed time instant from the

IGBT turn-on command. It is shown that the sensitivity is 500 mV per IGBT chip failure and the results are consistent under different operational and environmental conditions. As it is measured before the IGBT's turn-on threshold, $V_{GE(pre-th)}$ can be embedded within a standard PWM controller.

Table I. Examples of bond wire and chip failure detection techniques.

HSP	IGBT Type	Relative Sensitivity		Immunity to T_{vj} A/B	Reference
		Bond wire/chip failure (A)	T_{vj} (B)		
$V_{CE(on)}^{[1]}$	1-chip	1% (bond wire)	0.01%	100 (weak)	[29, 33, 34]
$V_{CE(on)}^{[2]}$	1-chip	14.6% (bond wire)	0.01%	1460 (strong)	[38]
$R_{CE(on)}$	2-chip	1.9% (bond wire)	0.44%	4 (weak)	[37]
$I_{G(peak)}$	2-chip	36% (chip)	0.05%	720 (strong)	[45-47]
dV_{CE}/dt	2-chip	25% (bond wire)	0.17%	147 (weak)	[35]

^[1] $V_{CE(on)}$ is the on-state voltage drop under load current.

^[2] $V_{CE(on)}$ is the on-state voltage drop at the inflection point.

II. COMPARISON OF EXISTING HEALTH MONITORING METHODS

Over the last two decades, many efforts have been dedicated to online bond wire failure detection of IGBT power devices. Most of the research focuses on the IGBT health sensitive parameters (HSPs) which can be measured externally through the main terminals – collector, gate and emitter (as well as Kelvin connectors where appropriate) – of an IGBT module. A selection of these methods is presented in Table I.

Table I shows five HSPs to determine bond wire failure ($V_{CE(on)}$, $R_{CE(on)}$, dV_{CE}/dt) and chip failure ($I_{G(peak)}$). A chip failure means the loss of all bond wires connected to one in a few chips in parallel. It is well known that the temperature dependency of a HSP can conceal their failure signature or depreciate their ability to detect a bond wire/chip failure. In order to determine the impact that T_{vj} has on the detection of bond wire failure and chip failure, the relative sensitivity for bond wire/chip failures and the relative sensitivity for T_{vj} are shown in Table I. The quotient of both indicates how immune each HSP is from T_{vj} changes. As HSPs are measured in different units - $V_{CE(on)}$ is measured in V, dV_{CE}/dt in V/s, $I_{G(peak)}$ in A and $R_{CE(on)}$ in Ω - a direct comparison of their sensitivity to temperature changes or to changes in the number of bond wire failure or chip failure is difficult. As such the sensitivity of each HSP must be normalized for comparison. Relative sensitivity is a normalized parameter and shown in (1). 'Variation' is either the T_{vj} reading of HSP for a given temperature above room temperature or the reading of HSP for a given number of bond wire or chip failures. 'Baseline value' is either the T_{vj} reading of HSP at room temperature or the reading of HSP where all bond wires or chips are healthy.

$$\text{Relative Sensitivity} = \frac{|\text{Variation}|}{\text{Baseline value}_{\text{room temperature}}} \times 100\% \quad (1)$$

In Table I, $R_{CE(on)}$ and dV_{CE}/dt have weak immunity. That is because both have the highest temperature-dependent HSPs with 0.44% and 0.17% respectively which causes challenges in

reading bond wire lift-offs. According to the references stated in the table, both techniques are not able to detect the first bond wire lift-off. $R_{CE(on)}$ is effective in determining the second bond wire lift-off whereas dV_{CE}/dt is only capable of detecting the fourth bond wire lift-off, and hence they cannot be regarded as good HSPs for single bond wire lift-off. $V_{CE(on)}$ measured at load current also has a weak immunity. However, $V_{CE(on)}$ measured at the inflexion point shows the strongest resistance to T_{vj} variation. Measurement of $V_{CE(on)}$ requires regrettably HV isolation, and the measurement circuit must deal with large V_{CE} voltage swings ranging from kilovolts during the blocking stage to a few volts during the on-state stage. $I_{G(peak)}$ has a strong immunity to T_{vj} changes but detecting a peak gate current value is difficult to implement practically. As gate currents are relatively small and measurements are taken close to the IGBT module the detection circuit must also deal with EMI challenges.

So far the techniques in Table I have only been applied to IGBT switches with only one or two chips. HSP will become more challenging when there are more IGBT chips in parallel, which are typical in multichip IGBT power modules. The main challenge is the increase in the complexity in the physics of failure as well as their characteristic formation, owing to the inhomogeneous power semiconductor chips combined with the heterogeneous construction of power modules. This can lead to an accelerate chip failure subject to operational stresses, which can depreciate the HSPs or conceal their failure signature. Multichip IGBT power modules are designed for large current ratings, and the number of chips connected in parallel depends on the chip current rating and the load current rating. The proposed method for detecting the IGBT chip failures in multichip HV IGBT power modules is presented next.

III. PRE-THRESHOLD VOLTAGE AS HSP

The gate-emitter circuitry comprises $R_{G(ext)}$, $R_{G(int)}$, C_{GE} and C_{GC} which form an RC circuit with V_{GG} as shown in Fig. 2. $R_{G(int)}$ and $R_{G(ext)}$ are the internal and the external gate resistors

respectively. C_{GE} and C_{GC} are the gate-emitter and gate-collector capacitors of the IGBT. V_{GG} is the gate voltage supply.

Fig. 2. RC circuit forming the waveform of V_{GE} from the PWM trigger event t_0 to $V_{GE(th)}$ during turn-on.

Eq. (2) describes the exponential rising of V_{GE} at turn-on before threshold voltage, $V_{GE(th)}$, which is reflected in Fig. 2 [48-50]. In Fig. 2, the off-state gate voltage supply, $V_{GG(off)}$, is -10 V whereas the on-state gate voltage supply, $V_{GG(on)}$, is +15 V. Thus the exponential rising of V_{GE} from t_0 to the threshold point at t_1 is due to the charging of the capacitive IGBT gate structure which is necessary prior to the IGBT module switching on.

$$V_{GE(pre-th)}(t) = (V_{GG(on)} - V_{GG(off)}) \left(1 - e^{-\frac{t}{R_G C_{ies}}} \right) + V_{GG(off)} \quad (2)$$

Where t is the time; R_G is the total gate resistance which includes $R_{G(int)}$ and $R_{G(ext)}$. C_{ies} is the gate input capacitance:

$$C_{ies} = C_{GE} + C_{GC} \quad (3)$$

Fig. 3. Representation of IGBT chip capacitances and internal resistances in multichip IGBTs.

In multichip IGBT power modules, each of the paralleled IGBT chips exhibits an inherent gate input capacitance and an internal gate resistance as shown in Fig. 3. Thus a healthy IGBT power module has an overall internal gate resistance, $R_{G(int),total}$ ($R_{G(int),total} = R_{G(int)}/n$), and gate input capacitance, $C_{ies,total}$ ($C_{ies,total} = (C_{GE} + C_{GC}) \cdot n$), with $R_{G(int),total}$ and $C_{ies,total}$ being the lumped resistances and capacitances by taking each parallel connected chip n into account. DIM800NSM33-F IGBT modules have a typical $C_{ies,total}$ of 144 nF and $R_{G(int),total}$ of 135 $\mu\Omega$ [43]. In the case of the total loss of bond wire connections to an IGBT chip, the effective inter-chip connection will be altered resulting in a corresponding decline in $C_{ies,total}$ and a rise in $R_{G(int),total}$. This partial open-circuit fault within the multichip module may not necessarily lead to an outright module breakdown, but will cause changes to its gate dynamic performance due to the $R_{G(int),total}$ and $C_{ies,total}$ changes with every chip failure and therefore the V_{GE} trajectory will be altered and the baseline value of $V_{GE(pre-th)}$ as defined in (2) and Fig. 2 will be shifted as shown in Fig. 4. A limitation of the proposed $V_{GE(pre-th)}$ method is that single bond wire lift-offs cannot be detected. This is because singular bond wire failures prior to outright chip failure will not cause changes to $R_{G(int),total}$ and

$C_{ies,total}$ because the chip is still connected and functional through the remaining bond wires. For this reason; it is the loss of all emitter bond wires connected to a chip which results in an outright chip failure that $V_{GE(pre-th)}$ can detect. Considering multichip power modules such as the DIM800NSM33-F IGBT power module which has 16 IGBT chips and each chip has 8 emitter bond wires resulting in 128 emitter bond wires in total, the loss of a single or few bond wires will not affect the operation at the rated current of the power module.

Fig. 4. Changes on V_{GE} with IGBT chip failures.

Fig. 4 shows that V_{GE} always starts from a fixed voltage level and as $V_{GE(th)}$ changes with chip failures, the trajectory of the V_{GE} will also change. Consequently, when measuring at a fixed point of time before $V_{GE(th)}$, the voltage level changes with the number of chips and this effect can be used as a HSP for IGBT chip failures. The HSP is therefore called the pre-threshold voltage $V_{GE(pre-th)}$. This knowledge allows the use of a simple counter that determines the point of measurement slightly before $V_{GE(th)}$ is reached. The counter will be triggered by the PWM signal to synchronise the measurement of $V_{GE(pre-th)}$.

Although IGBT power modules would continue to operate after the initial chip failures due to the paralleling of the chips, when more chips continue to fail, a warning status is reached that can be determined as critical. This means that beyond the loss of a certain amount of chips the power module will fail. The number of acceptable loss of chips depends on the application, and this decision lies with the customer. Generally, the loss of 10% of the silicon chips can be regarded as acceptable. Therefore, for the DIM800NSM33-F module, the detection of two chip failures out of sixteen has been set as the safety margin. Consequently, the experimentations discussed next are for the initial two chip failures of the DIM800NSM33-F.

IV. EXPERIMENTAL SET-UP

A purpose-built high voltage high current IGBT test rig was set up based on the schematic in Fig. 5 to investigate the proposed $V_{GE(pre-th)}$ method for detecting IGBT chip failures.

In Fig. 5, a 400 μH inductive load was utilised, and the DC-link supply voltage and current were set to 1800 V DC and 800 A DC respectively. The IGBT at the top is off at all times and is employed as an anti-parallel diode. The 16-chip IGBT module under test was pulsed from a gate driver with a voltage supply ranging from -10 V to +15 V. The gate driver used is the 2SC0535T2A1-33 from CONCEPT [51]. 3.9 Ω gate resistors for turn-on ($R_{G(ext),on}$) and 6.2 Ω gate resistors for turn-off ($R_{G(ext),off}$) were used between the ideal pulsed voltage supply and the IGBT gate terminal. The gate resistors used are thick

film surface mount resistors 1206 which are recommended in the gate driver datasheet, application note and manual [51-53]. The film surface mount resistors 1206 are typically used in gate driver circuits for real applications due to their low resistance tolerance of 1% and high-power proofing to minimize the gate-loop inductances (typical with wire wound resistors which could alter the switching performance of the IGBT [54]).

Fig. 5. Schematic for the $V_{GE(pre-th)}$ -IGBT chip failure tests.

A liquid temperature controlled heatsink was used to alter the IGBT power module's baseplate temperature T_C which in turn varies T_{vj} according to (4).

$$T_{vj} = T_C + P_D \cdot Z_{Th(jc)} \quad (4)$$

Where P_D and $Z_{Th(jc)}$ are the IGBT power dissipation and the thermal impedance between the IGBT junction and case, respectively. A settling time is required to fulfil $T_{vj} = T_C$. The IGBT baseplate temperature (T_C) was measured with thermocouples. The thermocouples used are Type K stainless steel washer probes with a tolerance of $\pm 1.5^\circ\text{C}$ [55]. In order to average out the thermocouple errors, six thermocouples were placed around the IGBT module mounting holes on the baseplate. For characterization, the IGBT V_{GE} waveform was measured by the oscilloscope to determine the best point of $V_{GE(pre-th)}$ measurement just before $V_{GE(th)}$. A photograph of the test rig is shown in Fig. 6.

Fig. 6. Photograph of the experimental set-up: complete test rig and IGBT close-up.

IGBT chip failure has been emulated by cutting off all the emitter bond wires of the IGBT chip. Consequently, the loss of 8 emitter bond wires connected to one chip which results in an outright chip failure is referred to as '1 chip loss' in the context. The loss of 16 emitter bond wires connected to two chips leads to the loss of two IGBT chips, which is referred to as '2 chip loss', and the healthy state before chip failure is referred to as

The corresponding author is Cuili Chen.

the 'baseline' in the experiments. An access hatch shown in Fig. 7(a) was developed in order to access the IGBT chips and cut off the emitter bond wires of one or two IGBT chips as shown in Fig. 7(b).

Fig. 7. Cutting off bond wires to impose IGBT chip failures: (a) Chip access hatch, (b) Close-up of bond wires cut off.

V. CHARACTERIZATION OF $V_{GE(pre-th)}$

Fig. 8(a) shows the experimental results of $V_{GE(pre-th)}$ for initial two chip failures on DIM800NSM33-F power module at T_{vj} of 20°C . Fig. 8(b) illustrates the measurement point of $V_{GE(pre-th)}$ using a fixed time delay of $1.2\mu\text{s}$ after V_{GE} starts rising from -10V . The results show that two successive IGBT chip failures of the sixteen-chip DIM800NSM33-F revealed a consistent trend on $V_{GE(pre-th)}$ that the voltage level $V_{GE(pre-th)}$ rises with every chip failure.

Fig. 8. (a) Changes in $V_{GE(pre-th)}$ with IGBT chip failures at 20°C , (b) Use of fixed time delay for $V_{GE(pre-th)}$ measurement at 20°C .

Fig. 9 shows that $V_{GE(pre-th)}$ is not affected by the switching transients of V_{CE} and I_C as the distortion of the uniform trend on V_{GE} occurs after $V_{GE(th)}$ when V_{CE} transient begins to fall and I_C begins to conduct/rise. Hence $V_{GE(pre-th)}$ has an advantage that it is not affected by the switching transients of collector-emitter voltage V_{CE} and I_C or changes in the load size.

Fig. 9. Clearance of $V_{GE(pre-th)}$ from I_C and V_{CE} switching noise at different IGBT health states.

In practice, the DC-link supply voltage ($V_{DC-link}$) is regulated to a 5% fluctuation [56]. Variations in the DC-link voltage levels impact on $V_{GE}(t)$ as shown in (5). However, the term dV_{CE}/dt in (5) remains zero until $V_{GE}(t)$ reaches $V_{GE(th)}$. At $V_{GE(th)}$, current starts flowing in the IGBT and dV_{CE}/dt becomes $dV_{CE}/dt \neq 0$ impacting on the voltage $V_{GE}(t)$. Therefore the proposed measurement is independent of DC-link supply voltage changes.

$$V_{GE}(t) = R_{G(int)} \left[C_{GE} \frac{dV_{GE}}{dt} + C_{GC} \frac{d[V_{CE} - V_{GE}]}{dt} \right] \quad (5)$$

A. Performance with respect to temperature changes

Eq. (2) shows that $V_{GE(pre-th)}$ is related to $R_{G(int)}$ which is a temperature sensitive parameter [11, 12]. Hence $R_{G(int)}$ can cause a variation on the gradient of the V_{GE} waveform when the IGBT chip temperature changes. $V_{GE(th)}$ is another temperature sensitive parameter that is related to $V_{GE(pre-th)}$ as depicted in Fig. 2. $V_{GE(th)}$ can be expressed [57, 58] as,

$$V_{GE(th)} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \quad (6)$$

Where V_{FB} is the flat band voltage, γ is the body effect parameter and ϕ_F is the Fermi energy which is given by:

$$\phi_F = \phi_T \ln \frac{N_A}{n_i} \quad (7)$$

with n_i as the intrinsic density, N_A as the substrate concentration, and ϕ_T as the thermal voltage:

$$\phi_T = \frac{kT}{q} \quad (8)$$

Where k is the Boltzmann's constant, q is the charge of an electron and T is the temperature. The intrinsic density n_i in (7) can be written as,

$$n_i = N_A e^{-\frac{E_g}{2kT}} \quad (9)$$

Where E_g is the energy gap.

Eqs. (8) and (9) show that the thermal voltage ϕ_T (8) and the intrinsic carrier concentration n_i (9) are temperature dependent parameters which account for the temperature dependency of $V_{GE(th)}$. The flat band voltage in (6) has also been reported as temperature dependent [28]. Consequently, when $V_{GE(th)}$ varies with temperature, it varies the gradient of the V_{GE} waveform which can influence $V_{GE(pre-th)}$.

Therefore, it is essential to investigate how $V_{GE(pre-th)}$ is influenced by the temperature and by the loss of chips. For this investigation, the temperature of the IGBT module has been varied through the heat plate. Tests at different temperatures are carried out before and after the chip failures. Fig. 10 shows the results of T_{vj} changes and the chip failures.

Fig. 10. Variation of $V_{GE(pre-th)}$ with IGBT chip failures at different temperatures.

The results in Fig. 10 show linear relationships between $V_{GE(pre-th)}$ and chip failures at each of the three temperatures. The results indicate that temperature variations do not affect the chip failure signature in $V_{GE(pre-th)}$. The reason is that gate-emitter voltage waveforms are very close with a small negative sensitivity of $-2.5 \text{ mV}/^\circ\text{C}$ when T_{vj} changes from 20°C to 100°C before the chip failure. The same observation is made when the power module lost one or two chips. Fig. 10 shows clearly that once the first chip has failed, there is a jump in the $V_{GE(pre-th)}$ level compared to the healthy module, with a positive sensitivity of $500 \text{ mV}/\text{chip failure}$ which is a significantly bigger change in voltage compared to the voltage change generated by the temperature as the T_{vj} sensitivity is only $-2.5 \text{ mV}/^\circ\text{C}$. Another $+500 \text{ mV}$ jump in $V_{GE(pre-th)}$ is detected when the second chip becomes disconnected with the bond wires. Consequently, it can be concluded that $V_{GE(pre-th)}$ is immune to T_{vj} changes as the change in $V_{GE(pre-th)}$ due to changes in T_{vj} is always lower compared to the voltage change caused by the disconnected chips. Based on Fig 10, a warning system for the power module tested can be easily implemented with a simple lookup table that holds the following information: $V_{GE(pre-th)} < 2.0 \text{ V}$ - power module is healthy (baseline); $2.0 \text{ V} < V_{GE(pre-th)} < 2.8 \text{ V}$ - one IGBT chip has failed; $V_{GE(pre-th)} > 2.8 \text{ V}$ - two IGBT chips have failed.

In Table I, $I_{G(peak)}$ is the only HSP for IGBT chip failure detection which can be compared with $V_{GE(pre-th)}$. Using (1), the relative sensitivity of $V_{GE(pre-th)}$ is 0.11% for T_{vj} and 28.7% for

chip failures. This compares well with $I_{G(\text{peak})}$ which has a strong immunity to T_{vj} with a T_{vj} relative sensitivity of 0.05% and the chip failure sensitivity of 36%. However, $V_{GE(\text{pre-th})}$ has been applied to multichip IGBT power modules (16-chip) whereas $I_{G(\text{peak})}$ was only applied to 2-chip IGBTs. The main advantage of $V_{GE(\text{pre-th})}$ over $I_{G(\text{peak})}$ is that $V_{GE(\text{pre-th})}$ employs a voltage sensor while $I_{G(\text{peak})}$ utilizes a current sensor. In general, voltage sensors are cheaper, simpler and lightweight compared to current sensors hence voltage-based HSPs are preferred from a practical perspective [48].

B. Changes in $R_{G(\text{ext})}$

$R_{G(\text{ext})}$ is one of the most influential components on $V_{GE(\text{pre-th})}$ according to (2). $R_{G(\text{ext})}$ is located on the IGBT power module's external circuitry and is temperature sensitive. For this reason, the impact of changes in $R_{G(\text{ext})}$ has been investigated.

The gate resistors employed for $R_{G(\text{ext})}$ have a temperature coefficient of resistance (TCR) of 100 ppm/K and thus the overall turn-on resistance changes from 3.9 Ω to 3.93 Ω for an 80 $^{\circ}\text{C}$ rise in temperature rise of the 3.9 Ω $R_{G(\text{ext},on)}$ utilized [54]. This effect was examined with the next available $R_{G(\text{ext},on)}$ of 3.96 Ω . The results in Fig. 11(a) depict a negligible impact on the chip failure signature of $V_{GE(\text{pre-th})}$.

Fig. 11. V_{GE} behaviour with changes in $R_{G(\text{ext})}$ and chip failures at 20 $^{\circ}\text{C}$.

Fig. 11(b) shows six $V_{GE(\text{pre-th})}$ measurements with $R_{G(\text{ext},on)}$ of 3.9 Ω and $R_{G(\text{ext},on)}$ of 3.96 Ω in the baseline, 1 chip failure and 2 chip failure conditions. The maximum error in the 3.9 Ω and 3.96 Ω measurements is only 4.5% and does not have an impact on the chip failure signature of $V_{GE(\text{pre-th})}$.

The sizing of $R_{G(\text{ext})}$ depends on the application. Fig. 11(b)

includes three $V_{GE(\text{pre-th})}$ measurements for 5% increase in $R_{G(\text{ext},on)}$ when it is physically changed to 4.27 Ω . The results show that only two chip failures can be detected as a $V_{GE(\text{pre-th})}$ reading of 1.42 V for the first chip failure falls within the baseline threshold and only the 2.2 V reading for two chip failures exceeded the baseline threshold. However, the $V_{GE(\text{pre-th})}$ reading of 2.2 V for two chip failures with $R_{G(\text{ext},on)}$ of 4.27 Ω is within the one chip failure threshold of $2.0 \text{ V} < V_{GE(\text{pre-th})} < 2.8$ for this power module. Hence the chip failure alarm is true, but the prediction is one chip failure rather than two chip failures which is false.

Consequently, it has been concluded that $V_{GE(\text{pre-th})}$ is highly dependent on $R_{G(\text{ext})}$. When the same $R_{G(\text{ext})}$ is utilised, the impact of temperature changes on $R_{G(\text{ext})}$ can be ignored. Whereas when $R_{G(\text{ext})}$ is physically changed, different $R_{G(\text{ext})}$ values will lead to different results, but the fundamental $V_{GE(\text{pre-th})}$ principle remains. Therefore any physical change of $R_{G(\text{ext},on)}$ by more than 1% requires a re-calibration of $V_{GE(\text{pre-th})}$.

C. Changes in V_{GG}

The impact of changes in the gate driver supply voltage, V_{GG} , has been investigated due to the relation with $V_{GE(\text{pre-th})}$ in (2). The gate driver used includes voltage regulation for a reliable $V_{GG(on)}$ to +15 V for IGBT turn-on, and -10 V ($V_{GG(off)}$) for IGBT turn-off is not regulated as it provides the compensation when $V_{GG(on)}$ fluctuates [53]. Eq. (2) shows a direct relation of $V_{GE(\text{pre-th})}$ with $V_{GG(off)}$. Consequently if $V_{GG(off)}$ varies, $V_{GE(\text{pre-th})}$ varies too. Given V_{GG} fluctuation, component tolerances and temperature dependence of the gate driver components, the impact of 2% and 5% error on -10 V $V_{GG(off)}$ resulting in -9.8 V and -9.5 V has been investigated.

Fig. 12(a) shows the voltage waveform for a 2% change in $V_{GG(off)}$ and Fig. 12(b) shows a comparison between 2% and 5% error compared to -10 V in $V_{GG(off)}$. Fig. 12(b) shows that there is enough margin in $V_{GE(\text{pre-th})}$ between every chip failure to allow signaling the detection of chip failures. Fig. 12(b) also shows repeatability in the context of changes in $V_{GG(off)}$ during two measurements. For example, if voltage fluctuations cause an error of 5% in $V_{GG(off)}$ during baseline condition, $V_{GE(\text{pre-th})}$ is in the order of 1.9 V following Fig. 12(b). This is 100 mV under the threshold margin that flags up 1 chip failure as described in section B above. If the voltage fluctuation disappears so that $V_{GG(off)}$ stabilizes back to -10 V and a chip has failed during that period then the second $V_{GE(\text{pre-th})}$ reading results in 2.1 V (from Fig. 12(b)). This value is within the reference to flag up 1 chip failure in the look-up table (2.0 V to 2.8 V). Consequently, the proposed circuit is immune to $V_{GG(off)}$ fluctuations up to 5%. If, however, a higher error is expected then a voltage sensor should be added to measure $V_{GG(off)}$. This information can then be processed to correct the value of $V_{GE(\text{pre-th})}$.

(a)

(b)

Fig. 12. V_{GE} behaviour with changes in V_{GG} and chip failures at 20 °C.

D. Repeatability

The previous sections have so far demonstrated the impact of $V_{\text{DC-link}}$, T_{vj} , $R_{\text{G(ext)}}$ and $V_{\text{GG(off)}}$ on the $V_{\text{GE(pre-th)}}$ measurement for one power module to determine chip failures. A second DIM800NSM33-F IGBT power module has been used to show if the proposed method produces the same results in terms of chip failure detection.

Fig. 13. Experimental results of $V_{GE(\text{pre-th})}$ on a different DIM800NSM33-F power modules at 20 °C.

Fig. 13 shows the measurement results conducted on two DIM800NSM33-F IGBT power modules (Modules A and B). Results at $T_{vj}=20^{\circ}\text{C}$ are portrayed in Fig. 13 where, for the same fixed time delay ($1.2\ \mu\text{s}$), the recorded errors are: 4.0% at baseline, 10.3% with 1 chip failure and 6.7% with 2 chip

failures. The small differences in errors show that $V_{\text{GE(pre-th)}}$ is repeatable based on the same decision statement used before: $V_{\text{GE(pre-th)}} < 2.0 \text{ V}$ - baseline; $2.0 \text{ V} < V_{\text{GE(pre-th)}} < 2.8 \text{ V}$ - 1 chip failure; and $V_{\text{GE(pre-th)}} > 2.8 \text{ V}$ - 2 chip failures.

VI. $V_{\text{GE(PRE-TH)}}$ PRACTICAL IMPLEMENTATION

On the premise of a known baseline value, two methods can normally be carried out for signal acquisition of the $V_{\text{GE}(\text{pre-th})}$ profile. Firstly, a snapshot measurement of $V_{\text{GE}(\text{pre-th})}$ can be taken at a fixed time instant corresponding to a pre-defined threshold value during the V_{GE} ramping-up. Alternatively, a fixed $V_{\text{GE}(\text{pre-th})}$ can be related to the lapse in time taken to reach $V_{\text{GE}(\text{pre-th})}$. The results obtained in this paper are based on the former method where the time is fixed and $V_{\text{GE}(\text{pre-th})}$ is measured.

Fig. 14. Schematic of $V_{GE(\text{pre-th})}$ measurement circuit for IGBT chip failure monitoring.

IGBT gate turn-on transients are in the order of hundreds of nanoseconds thus precise measurements necessitate a fast-respond triggering function and high bandwidth Sample-and-Hold (S/H) amplifiers to track the signal. Fig. 14 shows a simplified schematic of the hardware implementation for $V_{\text{GE(pre-th)}}$ measurement, which was embedded in the DIM800NSM33-F gate driver.

Fig. 14 shows the measurement points marked A, B, C and D where $V_{\text{GD(cs)}}$ (gate driver control signal), V_{GE} , $V_{\text{GE(pic)}}$ (V_{GE} analogue input to a programmable interrupt controller (PIC) for $V_{\text{GE(pre-th)}}$ measurement) and $V_{\text{GE(pre-th)}}$ signals are measured from respectively. The input buffer uses an operational amplifier (op-amp) to ameliorate the source impedance as the first stage in collecting $V_{\text{GE(pre-th)}}$. The buffer also prevents the $V_{\text{GE(pre-th)}}$ measurement circuit from loading the gate driver. In this way, the gate's normal operation is not affected, and thus the proposed $V_{\text{GE(pre-th)}}$ monitoring interface is suitable for online applications.

An edge detector is also shown in Fig. 14. The gate driver applies -10 V to maintain the off-state of the IGBT. Following a turn-on command, the gate input capacitance is charged by a +15 V gate voltage supply and V_{GE} starts to rise from -10 V. The edge detector is used to monitor the V_{GE} rising process and when it reaches -8 V, the edge detector sets off a delay counter in the PIC via a general purpose input-output (GPIO) pin on the

PIC. The PIC utilized is the PIC18F24K22 with a clock speed of 64 MHz. A delay of $1.2 \mu\text{s}$ has been predetermined to trigger the S/H circuit. After a $1.2 \mu\text{s}$ delay, an Analogue-to-Digital Converter (ADC) in the PIC measures $V_{\text{GE(pre-th)}}$. To allow the precise acquisition of $V_{\text{GE(pre-th)}}$ the PIC code enables the ADC module at the same time when the time delay counter is started by the edge detector and configures it ready to measure $V_{\text{GE(pre-th)}}$. When the $1.2 \mu\text{s}$ time delay is reached, the $V_{\text{GE(pre-th)}}$ sample is acquired immediately by the ADC. The $V_{\text{GE(pre-th)}}$ technique only requires a single sample at a time. Hence the fast-rising V_{GE} does not need to be tracked. If assurance is required, the proposed single $V_{\text{GE(pre-th)}}$ measurement process can be repeated. A lookup table is included in the PIC using a simple code with the $V_{\text{GE(pre-th)}}$ threshold values for different IGBT chip failure count. Thus the measured $V_{\text{GE(pre-th)}}$ value, as well as the ongoing chip failure count of the IGBT, are provided.

$V_{\text{GE(pre-th)}}$ is more pronounced in the V_{GE} region between the zero-crossing and 5 V which are within the voltage rating of the PIC pins. Thus a diode and Zener diode combination has been utilized as shown in Fig. 14 to allow only the V_{GE} portion between zero and 5 V to progress through to the PIC. This protects the PIC from overvoltage and negative voltage. Fig. 14 also shows galvanic isolation of the gate driver input as well as the $V_{\text{GE(pre-th)}}$ output. These isolation barriers are necessary to protect users as well as the associated low voltage components and equipment from the high voltage environment on the IGBT power module's collector-emitter circuit.

Fig. 15. Mode 1 waveforms of $V_{\text{GE(pre-th)}}$ applied during the on-state of the IGBT (duty cycle: 35%).

A. $V_{\text{GE(pre-th)}}$ measuring techniques

As the proposed V_{GE} measurement is before the threshold $V_{\text{GE(th)}}$, at which the IGBT switches on, $V_{\text{GE(pre-th)}}$ measurements can be conducted in two modes: Mode 1 is during the turn-on period that is signaled by the PWM controller, and Mode 2 during the off-state of the IGBT which is determined by the PWM signal. In both cases, the same information about the chip failure(s) can be detected.

1) Mode 1

This is when $V_{\text{GE(pre-th)}}$ measurements are collected online during the normal IGBT switching operation. The IGBT is thus driven normally and V_{GE} continues to its full gate voltage of 15 V of the normal duty cycle.

In Fig. 15 $V_{\text{GE(pre-th)}}$ of 1.8 V is successfully measured online in a typical PWM at 20 °C for a healthy power module. The frequency of the PWM is 1 kHz which is typically used in high voltage applications [59]. In each pulse, $V_{\text{GE(pre-th)}}$ is measured at the required time instant of $1.2 \mu\text{s}$ after V_{GE} starts rising from -10 V. The measured $V_{\text{GE(pre-th)}}$ is then available approximately $10 \mu\text{s}$ later after the measurement event which is caused by the processing time of the ADC employed. A faster ADC may be utilised, but this is not necessary because in health monitoring, wear out failures are gradual and slow compared to switching frequencies thus time can be afforded for processing and transfer of data to a host computer.

Fig. 16. Mode 2 waveforms of $V_{\text{GE(pre-th)}}$ applied during the off-state of the IGBT (duty cycle: 0.07%).

Table II. IGBT measurements with $V_{\text{GE(pre-th)}}$ circuit.

Lookup table (V)		$V_{\text{GE(pre-th)}}$ circuit		
		$V_{\text{GE(pre-th)}}$ (V)	Prediction	
		20 °C	100 °C	IGBT chip failure count
Baseline	$V_{\text{GE(pre-th)}} < 2.0$	1.86	1.71	0
1 Chip failure	$2.0 < V_{\text{GE(pre-th)}} < 2.8$	2.25	2.12	1
2 Chip failures	$2.8 < V_{\text{GE(pre-th)}}$	3.03	2.88	2

2) Mode 2

In this mode the PWM signal is low, and the IGBT is in the off-state. An interrupt routine which determines the health measurement overrides the off-status of the PWM signal and

triggers the gate driver with a duty cycle that allows only enough time to produce the required V_{GE} transient at which $V_{\text{GE(pre-th)}}$ is measured, and then turning off the IGBT. In this way, the status of V_{CE} and I_{C} is not affected: V_{CE} remains in the

blocking state, thus the switch never turns-on. This mode can be extended to test IGBTs during stand-by where for a longer period of time the devices are off. Fig. 16 shows such a premature V_{GE} pulse for testing $V_{GE(pre-th)}$ during the off-time of the IGBT. The pulse lasts only 2 μ s. Activation of this pre-mature pulse must be considered in the controller. Hence the test is only possible when the IGBT is in the off-state at the end of the pre-mature pulse and before the next PWM pulse. Fig. 16 shows the successful $V_{GE(pre-th)}$ measurement of 1.8 V at 20 °C for a healthy power module similar to Mode 1 above.

Table II shows the results using the $V_{GE(pre-th)}$ measurement circuit in Fig. 14. The measurements are conducted on different DIM800NSM33-F IGBT power modules from the same manufacturing batch as the modules tested in section V. The lookup table is derived from the characterization of the IGBT modules presented in section V. The results show successful implementation as the correct information about the chip failure count is obtained according to the lookup table.

VII. CONCLUSION

A new health sensitive parameter for IGBT chip failure monitoring in multichip IGBT modules was proposed. The method is $V_{GE(pre-th)}$ which takes place during the V_{GE} transient for turning on the IGBT. $V_{GE(pre-th)}$ is measured at a defined time instant between V_{GE} zero-crossing and the threshold voltage. $V_{GE(pre-th)}$ thus requires less hardware with only a voltage sensor and a counter. Practical results reveal a good $V_{GE(pre-th)}$ performance with IGBT chip failures with an average sensitivity of 500 mV per chip failure.

The hardware implementation of $V_{GE(pre-th)}$ has been

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The corresponding author is Cuili Chen.

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