ACTIVE GATE DRIVER AND SWITCHING CHARACTERISATION FOR HIGH-POWER IGBT MODULES

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Abstract

In modern power electronic systems, the Insulated Gate Bipolar Transistor (IGBT) power modules are the main workhorse and play a more and more important role. Their application fields include transportation traction, renewable energy systems, high-voltage electric power transmission systems and industrial motor drives. This thesis focuses on the IGBT module's dynamic characteristics and the state-of-the-art gate driving techniques. For the purpose of improving switching characteristics of high-power IGBT modules, candidate driving parameters for advanced active driving strategies are investigated and compared, and a novel current-source-based active gate driver is devised and experimental validated. To characterise the high-power IGBT modules and validate the effectiveness of the active gate driver, a double pulse test platform with wide testing conditions has been built with a generalised design procedure proposed. With the designed computer-aided software applied to the control and the data post-processing, both efficiency and accuracy of the test platform can be improved. Moreover, the transient current and voltage slopes controllability of high-power IGBT modules during turn-off transition is investigated. An effective and efficient evaluation method is proposed and validated for the module controllability assessment.

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I still remember the critical moment in my life when I obtained the opportunity of being a research student of my supervisor Dr. Bing Ji. I have always been grateful for his comprehensive guidance and support during my study. His encouragement stimulated me to overcome the difficulties in my research and daily life. I have learned from his pursuit of high-standard and persistence in research, which motivated me to be a lifetime learner and never stop to polish skills.

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List of Abbreviations

AC	Alternating Current
ACSGD	Active Current-Source Gate Driver
ADC	Analogue-to-Digital Converter
BJT	Bipolar Junction Transistor
CS	Current Source
CSL	Carrier-Storage Layer
CGD	Conventional Gate Driver
CCSGD	Constant Current-Source Gate Driving
CTE	Coefficient of Thermal Expansion
CMTI	Common Mode Transient Immunity
CMRR	Common Mode Rejection Ratio
DAC	Digital-to-Analogue Converter
DBC	Direct Bonded Copper
DC	Direct Current
DUT	Device Under Test
DPT	Double Pulse Test
EMI	Electro-Magnetic Interference
FPGA	Field-Programmable Gate Array
FS	Field-Stop
FWD	Free-Wheeling Diode
GPIB	General Purpose Interface Bus
GD	Gate Driver
GDA	Gate-driver Dominated Area
HV	High-Voltage

HF	High-Frequency
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IDA	Intrinsic-recombination Dominated Area
JFET	Junction gate Field-Effect Transistor
KVL	Kirchhoff's Voltage Law
LED	Light-Emitting Diode
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MOS	Metal-Oxide-Semiconductor
MTP	MOS-channel Turn-off Point
MCS	Mirror-structure Current Source
NPT	Non-Punch-Through
OCS	Op-amp-based Current Source
PWM	Pulse-Width Modulation
PCB	Printed Circuit Board
SOA	Safe Operating Area
TO	Transistor Outline
TVS	Transient Voltage Suppression
UVLO	Undervoltage-Lockout
VISA	Virtual Instrument Software Architecture
VVVF	Variable Voltage Variable Frequency
WBG	Wide Bandgap
ZCS	Zener-diode-based Current Source

CHAPTER 1

Introduction to Thesis

The power electronic system controls and regulates the electrical energy and makes it compatible to be utilised between sources and loads. The apparatus enabling this function is called the power electronic converter. The technical development of power electronics in the last 50 years has been significantly motivated by the increasing demand in energy conservation and utilisation in addition to prospective expectation globally for sustainable development. Those demands and expectations have elevated the status of power electronic techniques, meanwhile, bringing the requirements of high-reliability, high-efficiency, and low fabrication and maintenance costs into the converter system [1]. This chapter introduces the background, motivation, objective, and contribution of the thesis.

1.1 Overview of Power Electronics

A basic concept of power conversion incorporates a power stage and a control stage as shown in Figure 1-1. The power stage contains a matrix of power semiconductor switches with gate drivers attached and other passive components such as capacitors and inductors. This stage handles the power according to the commands delivered by the control stage. Digital processors at the control stage monitor the feedback information and send out control decisions to the executors via the gate drivers. Thus, the raw power at the input of a power converter can be regulated to generate the conditioned power at the output.

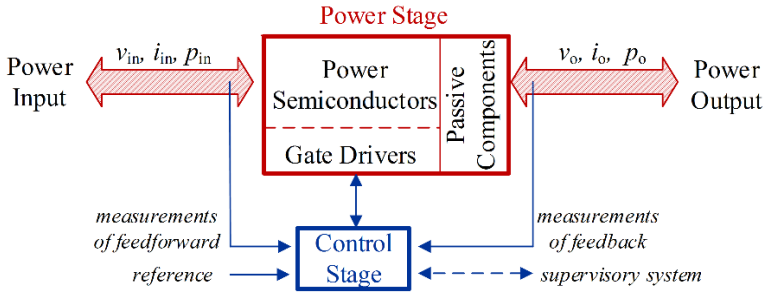


Figure 1-1: Outline of a typical power converter system [2].

Figure 1-2 shows commonly used power semiconductor devices. Thyristors can handle the highest power in electric grid, while the power metal-oxide-semiconductor field-effect transistors (MOSFETs) have the highest operation frequency for low- and medium-power applications, such as home appliances and electric vehicles. Insulated gate bipolar transistors (IGBTs) cover the widest range in both the power rating and the switching frequency, and are widely used in numerous industrial applications, such as the uninterruptible power supply, electric machine drives, renewable energy, and transport traction. These devices are mostly fabricated basing on silicon (Si) material. With the rapid development of wide band gap (WBG) semiconductors such as SiC and GaN, their application area can be further expanded to higher power and frequency usage.

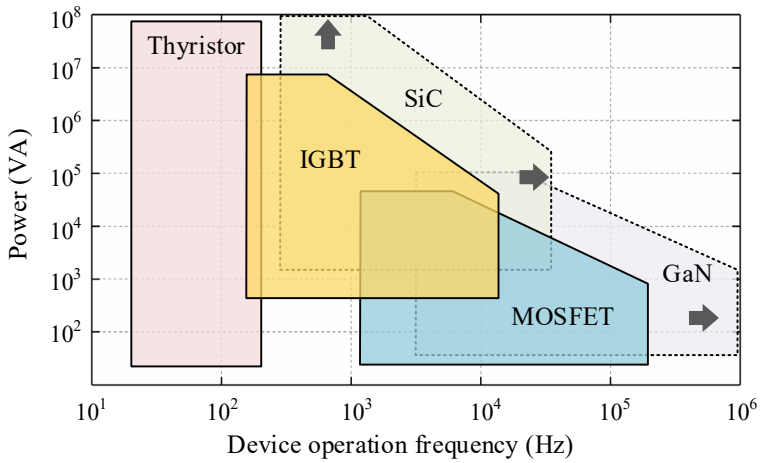


Figure 1-2: Typical power semiconductor devices and application range [3-5].

Semiconductor devices are specifically tailored during manufacturing to be utilised in applications, which lead to differentiated device types, power ratings, and even semiconductor materials. Taking silicon IGBT as an example, the fabrication process is illustrated in Figure 1-3. The silicon ingot is made from the raw material - sand, then the ingot is sliced into wafers. From silicon wafers, the IGBT chips are fabricated. These chips can be packaged solely or multiply into the discrete device or modular devices depending on the demand of power handling capability. The discrete device packed with the transistor outline (TO) package family types is usually used in low-power application, e.g. home appliance. To increase the current handling capability, multiple chips are configured in parallel to form a modular design as shown in Figure 1-3. Inside the standard power module, bond-wires and metal planes are used to realise the internal electrical connection among chips. Alternatively, the press-pack module applies pressure

contact to substitute the bond-wires with enhanced reliability. This unique structure facilitates the modules being stacked for series configuration. The modular design enables the IGBT devices to achieve a high-power rating above megawatts. In the following paragraphs, a typical application of a high-power IGBT module in a high-speed railway will be taken as an example to demonstrate its importance in the system.

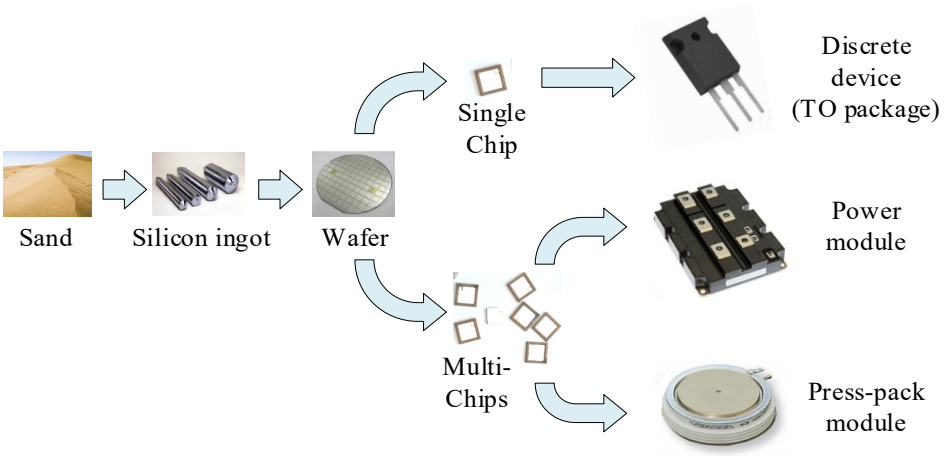


Figure 1-3: From sand to different power semiconductor devices.

With the trend of urbanisation, long-distance transportation with numerous populations moving between main cities is imperative. High-speed electric trains have been developed and widely deployed globally in recent decades, as shown in Figure 1-4. Meanwhile, this has stimulated the development and application of high-power semiconductor modules in power electronic converters.

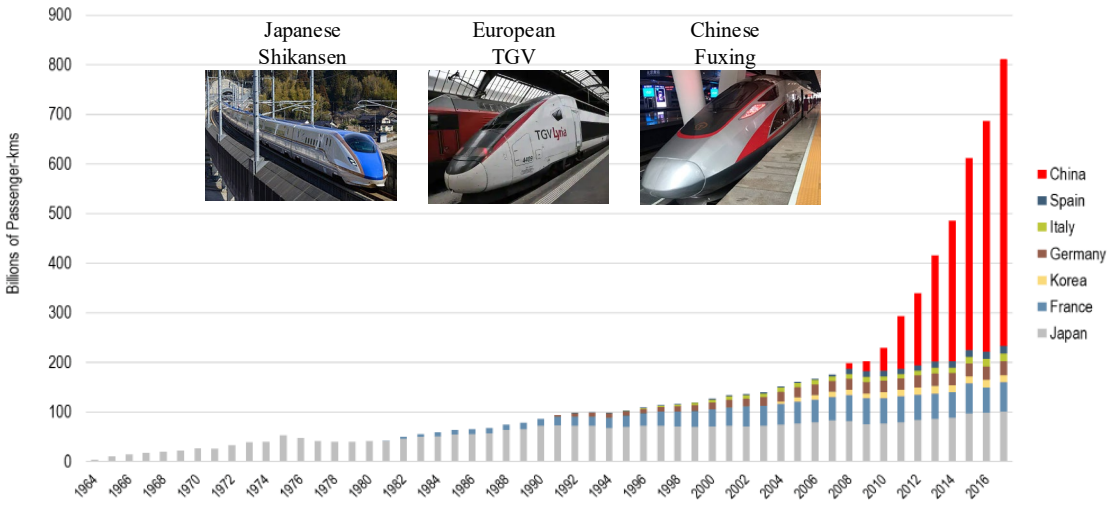


Figure 1-4: Development of high-speed railway 1964 – 2017 [6].

High-speed rail is advantageous compared with other usual transport methods, such as car and airplane. According to data in the literature [7], which compares the travel time of a 800km journey, the traffic volume of population per year, the fatal accident rate per billion kilometre, and the on-time rate, high-speed rail is shown to have an overall better performance than other modes of transportation.

Table 1-1 Comparison of different traffic modes [7]

	High-speed rail	Car	Airplane
Travel time (800km, h)	3.4	8.4	2.5
Traffic volume (million/year)	160	80	16
Fatal accidental rate (person/billion km)	0.0018	1.92	0.014
Travel on-time rate (%)	98	75	75

Environmental factors are also an inevitable consideration nowadays due to severe climate change. A comparison of the traffic modes including greenhouse gas emissions, energy source consumption, and noise can be obtained on the website of EcoPassenger [8]. The trip from London to Paris is taken as an example to demonstrate the benefits of a high-speed railway. It is clear that the high-speed rail is much more environmentally friendly compared with car and airplane.

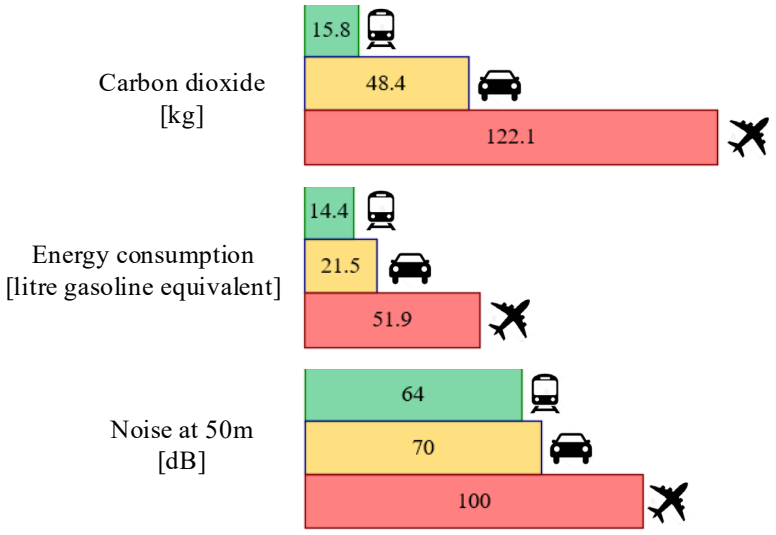


Figure 1-5: Comparison of traffic modes for a trip between London and Paris from environmental perspective, data provided by EcoPassenger [8].

Within high-speed rail, the high-voltage (HV) IGBT module plays a vital role in its energy system. It converts the electricity power from an alternating current (AC) power grid line

into the direct current (DC) link and is then inverted into AC power to drive the traction motor to supply the wheels located under all the passenger compartments.

The high-speed rail traction E-transformer designed by Alstom is shown in Figure 1-6. The 15kV, 16.67Hz AC power from the grid feeds the train's electricity, which has cascaded via the IGBT-module-based converter on the line side to convert the input frequency to 5kHz. The higher frequency effectively reduces the size and weight of the transformer. Then, the IGBT-module-based converter on the secondary side regulates the power to the 1650V DC-link to feed the propulsion drive. In this design, the IGBT modules with 6.5kV and 3.3kV blocking capability are implemented.

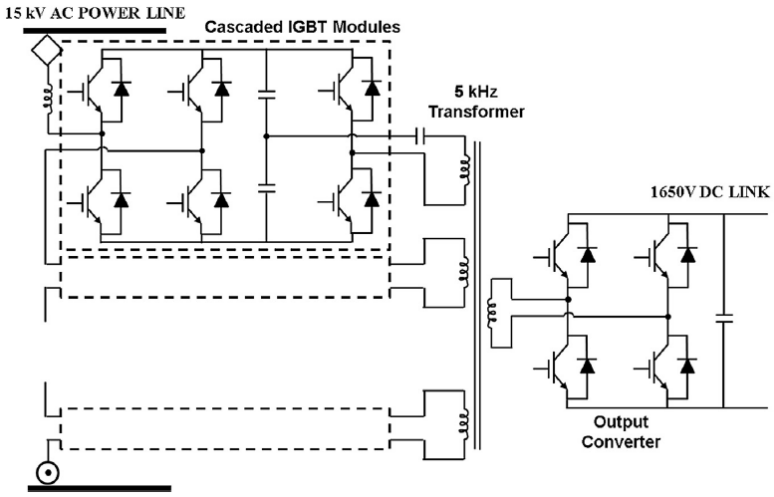


Figure 1-6: Configuration of high-speed rail traction E-transformer by Alstom [9].

Another example in Figure 1-7 demonstrates the traction converter in the Shinkansen N700 series, which consists of a 3-level pulse width modulation (PWM) converter and a variable voltage variable frequency (VVVF) control system inverter. It relies on the IGBT-module-based converter to realise the AC-DC-AC electricity conversion. IGBT modules with 3.3kV/1.2kA ratings are used, and the system is designed to drive four traction motors simultaneously.

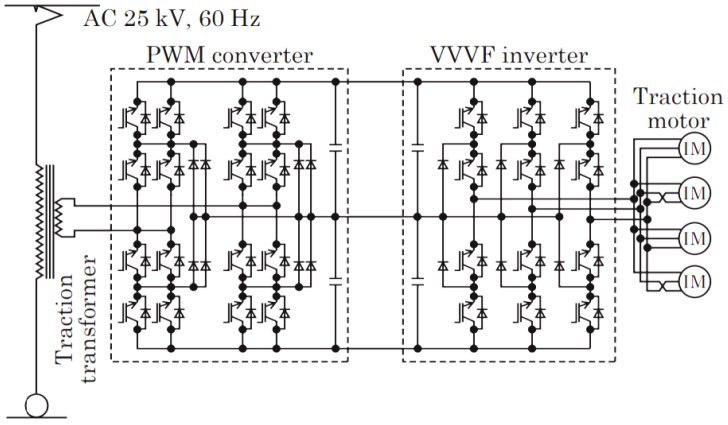


Figure 1-7: Configuration of series N700 Shinkansen traction converter [10].

From the above examples, the power electronic technique relies on the switch-mode power converters to handle and regulate the electricity, where power semiconductor devices behave like single-pole single-throw switches. Ideally, the switch withstands voltage across it without passing current when it is open (off-state), otherwise it conducts current without voltage drop on it when it is closed (on-state).

Power devices normally switch at a frequency ranges between kilohertz and megahertz, in other words, the switching period could go from micro-seconds to milli-seconds. The concepts of static characteristics and dynamic characteristics of power devices are depicted in Figure 1-8. For most cases, the static on and off states together take the most time of a single switching period, while the dynamic turn-on and turn-off transitions could be completed within a much shorter duration. When the load current flows through the switch at the static on-state, a few volts dropping across the switch could exist in practice. Hence, the conduction loss is generated. At the static off-state, the energy loss generated on the switch is negligible due to the extremely small leakage current. It should be noted that, at the dynamic transitions in both turn-on and turn-off, the product of current and voltage waveforms on the switch corresponds to switching loss.

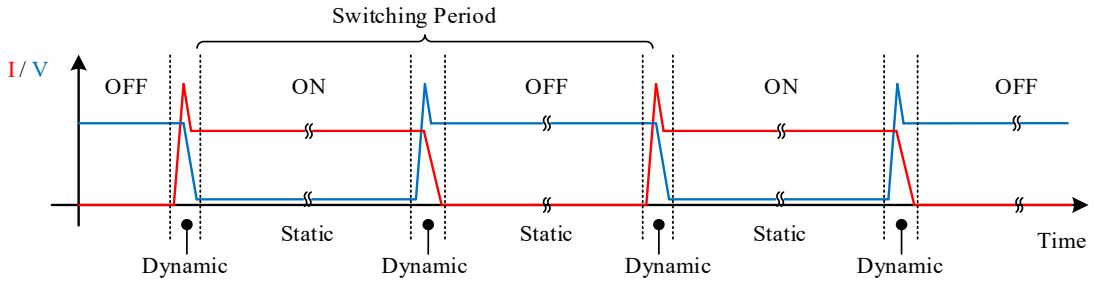


Figure 1-8: Static characteristics and dynamic characteristics of semiconductor switch.

Energy efficiency, which simply means consuming less energy to perform the same task, is an important factor in power electronic applications. Both conduction and switching losses generated from a power device contribute to the overall converter losses [11]. The total energy loss on a power device in one switching cycle is given by Equation (1-1)

$$E_{total} = E_{con} + E_{sw} = E_{con} + E_{on} + E_{off} \tag{1-1}$$

where E_{con} is the static conduction energy loss, and E_{sw} is dynamic switching energy loss, which is equal to the sum of turn-on loss E_{on} and turn-off loss E_{off}.

Similar to Equation (1-1), from the average power perspective, the total power loss can be expressed as Equation (1-2)

$$P_{total} = P_{con} + P_{sw} = V_{CE(on)} \cdot I_C \cdot D + (E_{on} + E_{off}) \cdot f_{sw} \tag{1-2}$$

where $V_{ce(on)}$ is the on-state voltage drop on IGBT, I_C is the collector current flowing through IGBT, D is the duty cycle, and f_{sw} is the switching frequency of the device.

As shown above, the conduction power dissipation is dependent on the duty cycle, while the turn-on and turn-off power losses are dependent on the switching frequency. Thus, a higher switching frequency could increase the proportion of the switching loss in the total power consumption on the device. In application, a higher switching frequency is generally desired due to substantial reductions in the size and weight of reactive components required to filter the harmonics at output [12].

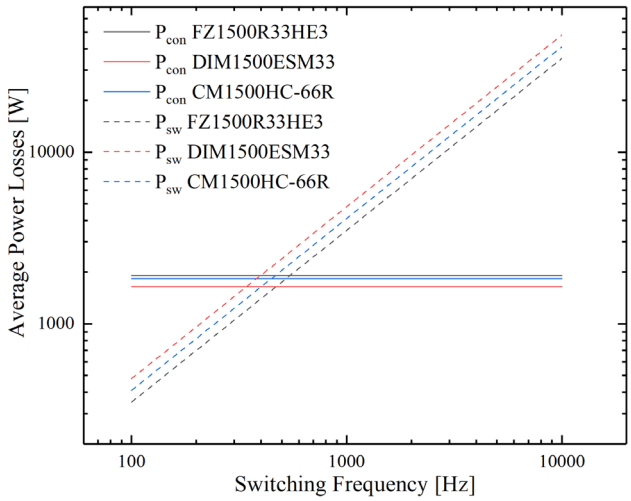


Figure 1-9: Power losses against switching frequency of three IGBT modules in logarithm scale.

A general comparison between P_{con} and P_{sw} against f_{sw} of three IGBT modules with 3.3kV/1.5kA ratings is presented in Figure 1-9. Parameters from manufacture datasheets under the testing conditions of 1800V, 1500A, and 25°C are used for calculation, with an assumption of 50% duty cycle. It is that P_{sw} becomes the dominator rather than P_{con} when f_{sw} rises above 400Hz approximately, whereas P_{con} is higher at lower switching frequency. Therefore, the device's dynamic performance draws more and more attention, because of the preference in the high frequency operation, as well as the boost in maximum switching speed that the latest generation of semiconductor devices can reach, which is driven by adopting the WBG material to replace silicon. Overall, reducing energy loss of power module benefits the efficiency of energy utility, the temperature stress on the device, and the thermal management of converter systems.

To operate power semiconductor devices, the gate driver is an essential circuit attached to the device peripherally, as shown in Figure 1-10. It is located between the control stage and power stage to provide electrical isolation, as well as driving energy to turn the switch on and off following the control signal [13]. The most important capability of the gate driver is that it has an impact on the static and dynamic characteristics mentioned above.

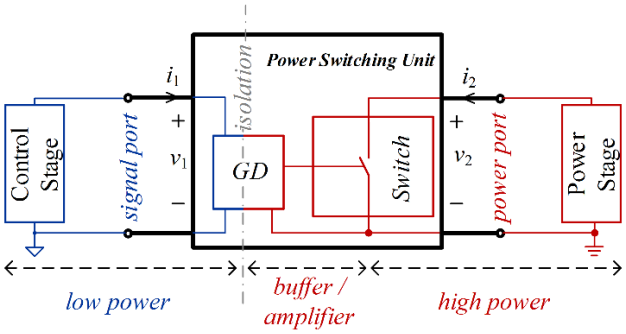


Figure 1-10: Simplified two-port switch unit including a power switch and a gate driver [2].

1.2 Research Motivation

Global competitive marketplaces require improvements in operational efficiency, in-service reliability, in addition to lower fabrication and maintenance costs of power electronic systems. Achieving these goals will be difficult if it depends on the system-level design of a converter alone. Attention should be paid to the fundamental elements of converters: the power semiconductor devices and its peripheral driving circuit.

The high-power IGBT modules process large amounts of electrical energy in their application scenario and are exposed to complex operational conditions such as electrical stress variants, environmental changes, and health degradation. According to an industry-based survey presented in paper [14], the semiconductor device is the most frangible component of a power electronic system, having been selected by 31% of respondents. This is much higher than the subsequent component “capacitors” (17%). Figure 1-11 depicts the main differences between ideal and practical hard-switching waveforms of IGBT. It can be seen that the switching delay, overshoots, switching and conduction losses all exist in practice, thereby causing problems.

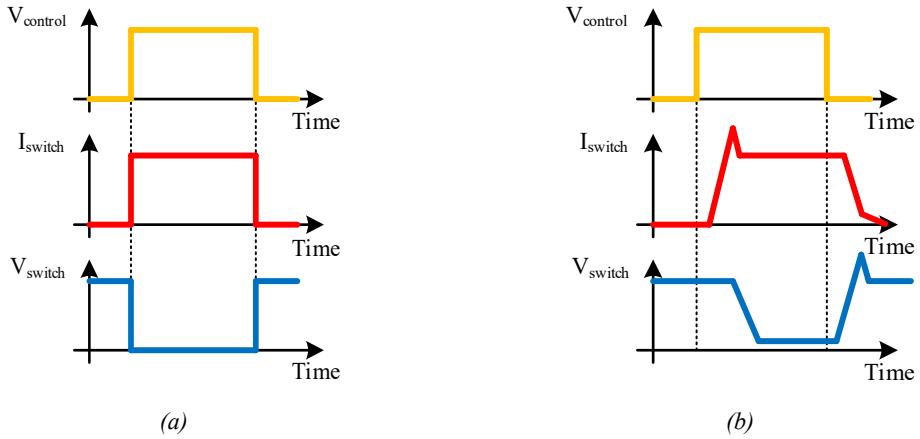


Figure 1-11: Voltage and current switching waveforms of ideal and practical power switches.

The latest development of active gate driver techniques enables a higher system efficiency by reducing the switching losses to some extent, without threating the reliability of power modules. The switching transient of IGBT is significantly affected by its gate driver parameters. When compared with the conventional fixed driving circuit and fixed parameters (i.e. gate resistance), the active gate driver can be more flexible and realise the optimal switching trajectories under the varying load conditions. For instance, when the IGBT is under low current load, it can be turned on fast to reduce the losses. Furthermore, when the current stress is high, the device should be turned on slowly to avoid destruction from the current overshoot.

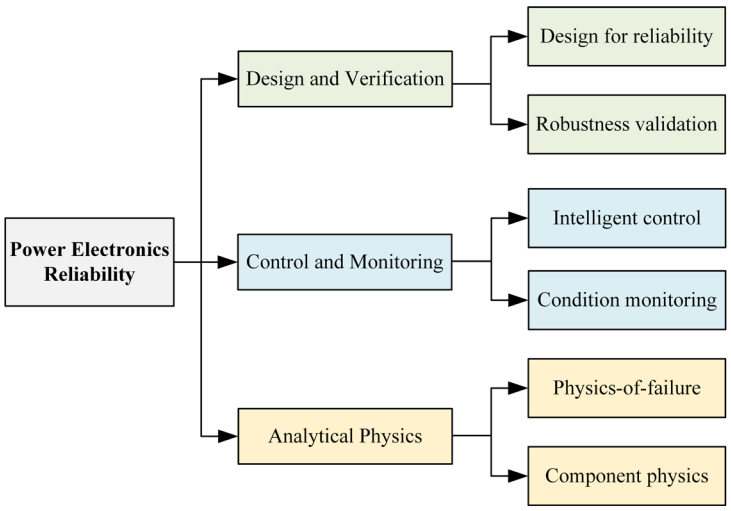


Figure 1-12: Categories of power electronics reliability research needs concluded by researchers [15].

The power electronics reliability research involves three main categories as concluded in paper [15]: 1) physical analysis to understand the root reasons and mechanism in failure;

2) design for reliability and robustness validation process to enhance the reliability of products during each development process; and 3) the control and monitoring techniques to ensure the reliable field operation under specific conditions, as shown in Figure 1-12. Much effort has been undertaken focusing on the failure mechanism and condition monitoring techniques of the IGBT module. Nonetheless, the intelligent active control, which works as the execution unit to take appropriate actions according to the information from failure and condition monitoring, is an emerging concept and immature technique. For the traditional power electronics converters, the IGBTs are controlled by a main controller, and the controller is galvanically isolated by the driving circuit from the power modules. Therefore, it is unfeasible for this main controller to gather the information from monitoring circuits quickly and have a swift response (i.e. when short circuit occurs, the IGBT must be turned-off in a few microseconds). Thanks to the development of microelectronics and manufacturing, the cost of microcontrollers has been reduced rapidly, thereby that enables an additional controller to be added into the driving circuit to realise localised intelligent control for the IGBT. The prediction of failure and protection of overstress will effectively enhance the reliability of the power electronic systems.

The intelligent active gate driver is more demanded by high power IGBT modules which merit the cost increase by applying an additional microcontroller to improve the reliability and efficiency. Moreover, the switching transition of high power IGBT modules takes longer than low power devices, thus giving more room for control loop design to overcome the signal propagation delays in electronic circuits.

In summary, the main motivation of this project is to further improve the performance of the IGBT module and exploit its full potential, in addition to increasing its reliability during operation and protect this important and expensive power semiconductor device to avoid catastrophic failure.

1.3 Objectives and Contributions

The aims of this research work are to:

- Obtain a comprehensive understanding of the theoretical and physical principles behind the static and dynamic characteristics of high-power IGBT modules and their correlations to the gate driving circuit including both conventional and current-source drivers.
- Provide an overview of state-of-the-art techniques in gate driving for power semiconductor devices.
- Design a novel and specific active driving circuitry for a high-power IGBT module to realise switching transient characteristics optimisation.
- Design a cost-effective double pulse test platform for high-power modules with a wide range of testing conditions including operating voltage, operating current, and operating temperature.
- Accurately measure the desired characteristic parameters of the device under test and post-process the data exported in an efficient and accurate way.

All the objectives are covered in the thesis, and the novel contributions to knowledge are highlighted below:

- The driving parameters can be used to refine IGBT dynamic behaviours are comprehensively investigated and assessed.
- Novel current-source-based active driving circuitry for high-power IGBT modules is developed.
- A new and generalised design method of the double pulse test platform with wide testing capability and cost-effectiveness is provided.
- The turn-off transient controllability problem of high-power IGBT modules is investigated, with a new assessment method proposed.

1.4 Thesis Structure

In CHAPTER 1, the background of power electronics and motivation for this project are introduced. CHAPTER 2 gives a detailed discussion on the high-power IGBT modules from chip to packaging techniques with its static and dynamic behavioural model derived. CHAPTER 3 introduces the gate driver unit of high-power IGBT modules together with a review of the state-of-the-art active driving techniques. To characterise the switching

and conducting performance of the module and the impacts of the gate driving parameters on it, a wide-range 3.3kV module testing platform is designed with a generalised design method proposed in CHAPTER 4. In CHAPTER 5, the driving parameters that can be used in an active gate driver are analysed and compared, and the novel current-source-based active gate driver is described in detail. CHAPTER 6 investigates the controllability problem in high-power IGBT modules under various conditions, and a practical method for fast evaluation is proposed. Finally, CHAPTER 7 summarises the research and gives a suggestion for future work to enhance the proposed techniques.

CHAPTER 2

High-Power IGBT Modules

In this chapter, the details of high-power IGBT modules are introduced covering semiconductor structure, module packaging, static and dynamic characteristics. A comprehensive behavioural model of IGBT module during switching transients is derived, which bridges device's dynamic characteristics and peripheral driving circuit. In addition to the conventional gate driver (CGD), the analytical expressions of characteristics under a current-source driving are also provided.

2.1 IGBT Chip Structure

After about thirty years of continuous development, IGBTs are now widely used power devices and the workhorse of medium- and high-power industrial applications, because of their properties of high input impedance, good controllability of switching speed and rugged operating capability [16].

The basic structure of an IGBT semiconductor cell is illustrated in Figure 2-1, which includes some important equivalent components highlighted. A highly doped n^+ layer is attached with aluminium to form the emitter terminal, which is contained by a *p*-doped well. A gate terminal is embedded into the SiO_2 insulation layer. When sufficient positive gate-emitter voltage is applied, an electron channel under the gate oxide is formed, which bridges the n^+ and n^- drift regions through the well, to allow electrons flowing from emitter to collector, hence the IGBT is on.

To compare with the power MOSFET, the IGBT has a similar structure except an additional highly doped p^+ region connecting between the n^- layer and collector terminal [12]. This modification induces the conductance modulation effect [3], which effectively reduces the on-state voltage drop across the IGBT to further reduce the conduction power loss of device. The function of p^+ layer is to inject holes into the n^- drift region, that leads

to numerous electrons moving from highly doped n^+ region into n^- region for maintaining electric neutrality. Thus, the impedance is decreased owing to the inflow of free carriers to the low-doped n^- layer.

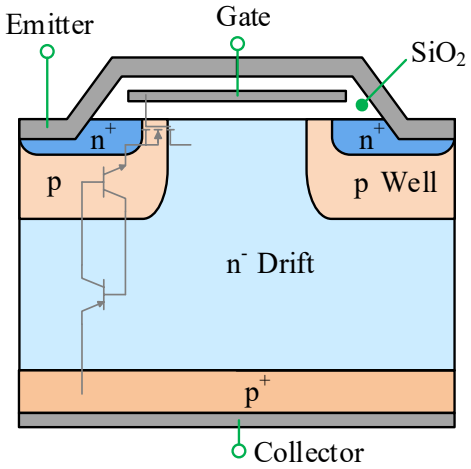


Figure 2-1: Basic IGBT semiconductor cell structure.

However, the new layer construction forms the equivalent *npn* and *pnp* transistors inevitably. These two transistors combine together to form a thyristor, which brings the possibility to the device to be latched up during stationary operation or turn-off as long as some conditions are satisfied [5]. Some measures, e.g. short-circuiting the base and emitter of *npn* transistor or reducing ohmic resistance [3], are necessary to be taken when designing and fabricating the IGBT to avoid the latch-up phenomenon, which might result in loss of controllability of the device and fault in the converter system using it.

Additionally, another issue brought by the new layer construction is the current tailing [12], which increases the turn-off transition time and contributes more switching power loss. When turning the IGBT off, the effective MOSFET part can be switched off immediately, but the current in the *pnp* part keeps flowing due to the stored minority charge carriers in the drift region, which are recombined in a relatively slower speed (i.e. tail current) to prolong the time required up to tens of microseconds for the IGBT current reducing to zero.

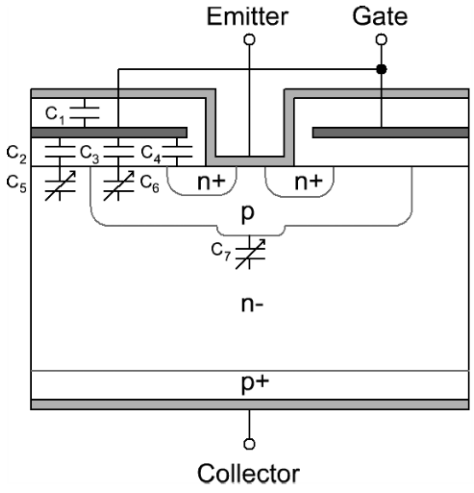


Figure 2-2: Parasitic capacitances of the IGBT [3].

Several lumped parasitic capacitors, including C_{GE}, C_{GC}, and C_{CE}, are formed in the IGBT cell due to its physical structure, and the detailed distribution is indicated in Figure 2-2. Generally, C_1, C_2, C_3 and C_4 are formed between gate terminal and emitter terminal, drift layer, *p*-well layer, and n^+ layer, respectively. It is crucial that the capacitance of C_5, C_6 and C_7 are voltage-dependent, because they are determined by the length of space-charge field. Hence, the three lumped parasitic capacitors can be represented below.

$$C_{GE(v)} = C_1 + C_4 + \frac{1}{\frac{1}{C_3} + \frac{1}{C_{6(v)}}} \tag{2-1}$$

$$C_{GC(v)} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_{5(v)}}} \tag{2-2}$$

$$C_{CE(v)} = C_{7(v)} \tag{2-3}$$

According to the analysis of IGBT basic structure, its simplified equivalent circuit model can be derived as shown in Figure 2-3 (a). Since measures are carefully taken to eliminate the latch-up problem in modern IGBT design, the equivalent *npn* transistor can be omitted [17].

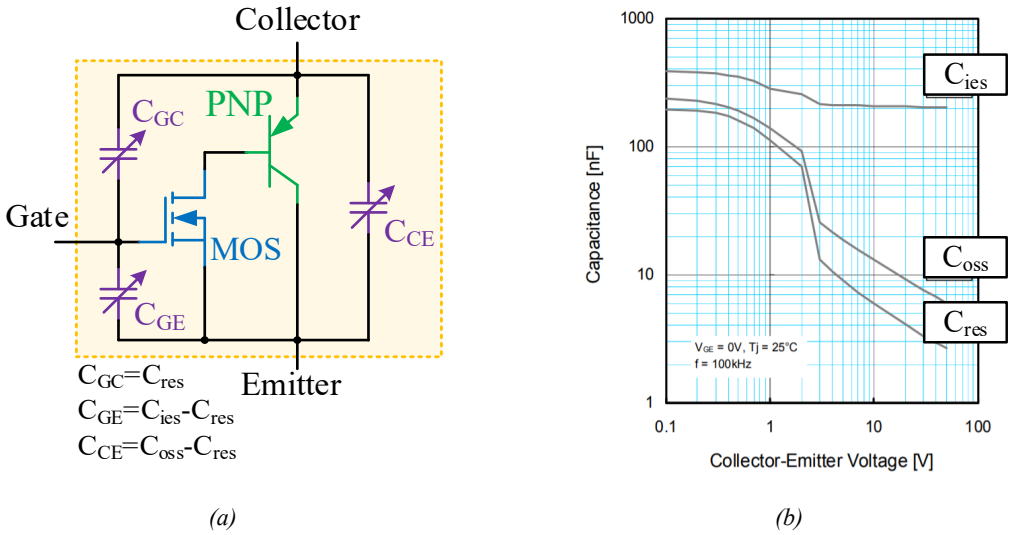


Figure 2-3: IGBT model (a) equivalent circuit; (b) exemplificative capacitance of module CM1500HC-66R.

Different application scenarios lead to different structural optimisation criteria. On-state voltage is a vital parameter for IGBT modules in high-speed rail traction due to the relatively low frequency of inverter [18]. The structural evolution of HV-IGBT chip cell is illustrated in Figure 2-4.

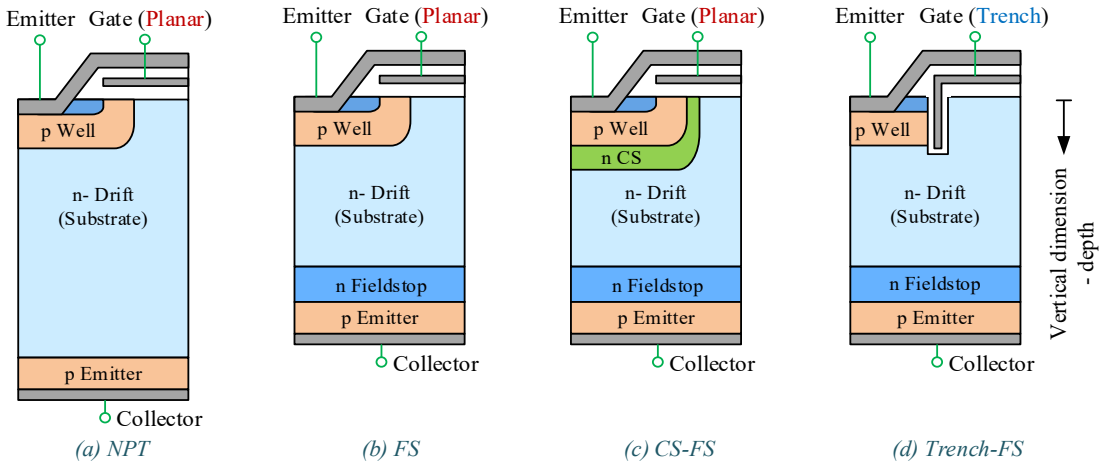


Figure 2-4: Semiconductor structural evolution of high-voltage and high-power IGBT chip.

The basic cell structure as descripted before is also known as non-punch-through (NPT), which requires thick drift layer for high-voltage blocking capability. To reduce the on-state voltage drop, a buffer layer called field-stop (FS) or similar concepts from different companies known as soft punch-through or light punch-through [19, 20] is implemented. Further conduction voltage improvement can be achieved by inserting a carrier-storage

layer (CSL) with heavy doping around the *p*-well to optimise the on-state charge carrier distribution [21-23]. Alternatively, efforts can be made on the structure of gate terminal to reduce on-state voltage. The trench structure leads to several changes in device's characteristics. Firstly, it eliminates the junction gate field-effect transistor (JFET) effect between cells in planar design to increase the conductivity. Secondly, the vertical structure realises the increment of cell density, which means more cells can be paralleled to lower the on-state resistance. Thirdly, the on-state carrier distribution in drift region is changed, which has a higher carrier concentration on the emitter side as depicted in Figure 2-5 [24, 25].

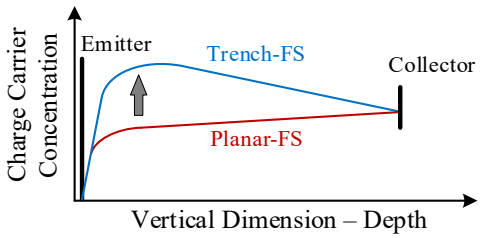


Figure 2-5: Typical on-state carrier distribution of trench and planar gate designs.

Current commercially available HV-IGBT modules with their chip technologies and manufactures are summarised in Table 2-1. The gate structure is evolving from the planar to the trench. The modification of on-state charge carrier distribution reduces the conduction voltage of IGBT but could result in the uncontrollable *di/dt* or *dv/dt* during switching transients. This problem will be discussed and experimentally investigated in CHAPTER 6.

Table 2-1 Summary of high-voltage IGBT modules technologies and manufactures in market

Voltage Class	Chip Technology	
	Planar	Trench
3.3kV	Mitsubishi; Hitachi; Dynex; ABB	Mitsubishi; Hitachi; Infineon; Dynex (*2019*); ABB (*2018*); Fuji
4.5kV	Mitsubishi; Hitachi; Dynex; ABB	Mitsubishi; Hitachi; Infineon; Dynex (*2019*)
6.5kV	Mitsubishi; Hitachi; Dynex; ABB	Mitsubishi; Hitachi (*2018*); Infineon; Dynex (*2019*)

2.2 IGBT Module Packaging

Although semiconductor chip is the core element of power device, the packaging technique also plays a vital role and must not be ignored. The chip itself is hardly to be applied in the electrical circuit, which requires the packaging to provide the electrical connection for both of internal and external circuits, the thermal interface for heat dissipation, and the ambient protection from mechanical, chemical, and electromagnetic environments. Internal electric interconnections among chips are realised by copper planes and aluminium bond wires. External power terminals are assembled with metal busbar for high current handling. Moreover, the heat generated during the operation of device needs to be cooled down effectively to guarantee the performance of power devices, which challenges both the module layout design and packaging materials. Last but not least, a rigid and insulated outer housing is required to encapsulate the module for safety and reliability purposes.

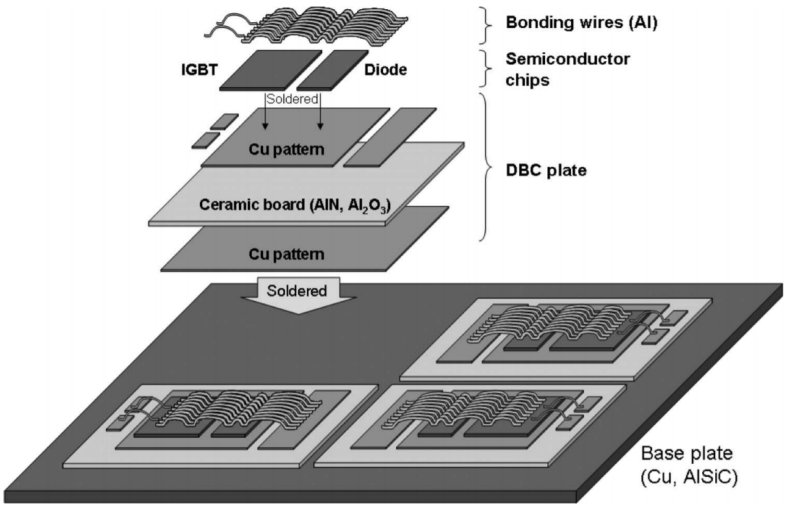


Figure 2-6: Conventional internal structure of IGBT power module [26].

The internal structure of conventional IGBT module is shown in Figure 2-6. The semiconductor chips of IGBT and free-wheeling diode (FWD) are soldered on the top-side copper pattern of direct bonded copper (DBC) plate. The DBC substrate is normally constructed on an isolated ceramic tile with a sheet of copper bonded on both sides, which provides the interconnections for electric circuits, the good thermal conductivity for cooling, and high voltage isolations. Multiple substrates are soldered onto the base plate, and the aluminium bond wires are utilised for electric connections. The plastic housing is

glued on the base plate to provide mechanical protection as the outer case, with silicone gel filled in to enhance the dielectric.

Table 2-2 lists the commonly utilised materials in the semiconductor module package. Apart from the electrical conductivity, the thermal characteristics of these materials are also crucial for packaging design, such as thermal conductivity and coefficient of thermal expansion (CTE). Good thermal conductivity improves the heat dissipation capability of module, while the mismatching of packaging materials might lead to reduced reliability, e.g. the bond wire lift-off [27].

Table 2-2 Materials for power module packaging and important coefficients

	Material	Heat conductivity [W/(m*K)]	Thermal expansion coefficient [10^{-6}/K]	Electrical conductivity [10^7S/m]
Bond-wire	Al	230	22.5	3.8
Semiconductor chip	Si	148	4.1	--
DBC pattern	Cu	394	17.5	5.9
DBC ceramic substrate	AlN / Al_2O_3	180 / 24	5.7 / 8.3	Insulator
Solders	Solder	~70	15 - 30	0.9
Base plate	Cu / AlSiC	394 / 180	17.5 / 7	5.9 / --
Power terminals	Cu	394	17.5	5.9
Housing	Plastic	--	--	Insulator

Considering the external appearance and dimension of module packaging, products from different manufactures would not present significant dissimilarity, that provides ease of assembly to users. Figure 2-7 displays some typical appearance of high-power modules. The A-type is mainly applied for 3.3kV semiconductor chips, which normally has a maximum isolation voltage V_{iso} above 6kV. The B-type has highest dielectric level with V_{iso} reaching above 10kV, this type of package is mainly used for semiconductor chips ranging between 4.5kV and 6.5kV. The C-type packaging is the next-generation standard packaging for high-voltage modules (either Si or SiC devices), which provides effectively lowered internal inductance and improved power density. Its innovation in scalability and

robustness will greatly simplify the system design and manufacturing and enhance the long-term reliability in application.

Figure 2-7: Typical appearance and dimension of high-power module packaging.

Inside the module package, internal chips and external terminals can be configured to various electrical circuits targeting different application scenarios, which are shown in Figure 2-8. The configurations of the single switch and the half-bridge are the most common.

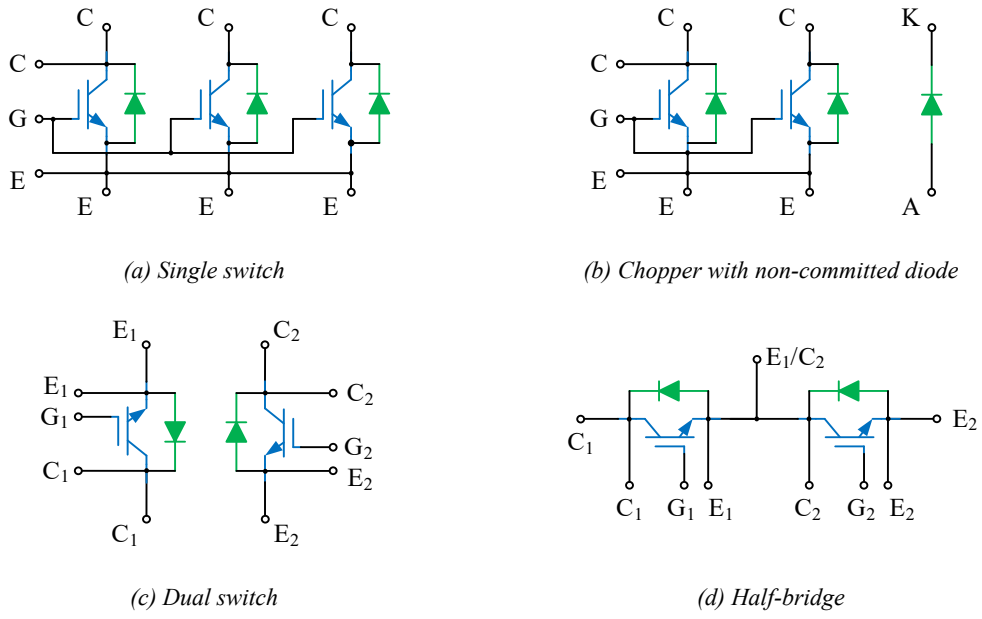


Figure 2-8: Typical internal and terminal configurations of high-power module packaging.

Module packaging inevitably introduces parasitic inductance and capacitance due to the inductive conducting traces and the capacitive coupling between the top traces on DBC

and baseplate. For Si-based device, the module inductance draws much attention in terms of voltage overshoot and oscillation, while the parasitic capacitance of packaging is often ignored. However, due to the extreme fast current and voltage commutation in WBG devices, both inductance and capacitance play important role. The displacement current governed by *dv/dt* appearing across the capacitance worsens the electromagnetic interference (EMI) performance and diminishes the switching loss [28]. Therefore, the compromise among the parasitic capacitance, the stray inductance, the thermal performance, and the cost will be the challenge for future packaging design.

2.3 Static Characteristics

The typical output characteristics of the IGBT with anti-parallel FWD is shown in Figure 2-9. It can be divided into four regions for discussion, which are the cut-off region, the saturation region, the inverse region, and the active region [3, 5, 18].

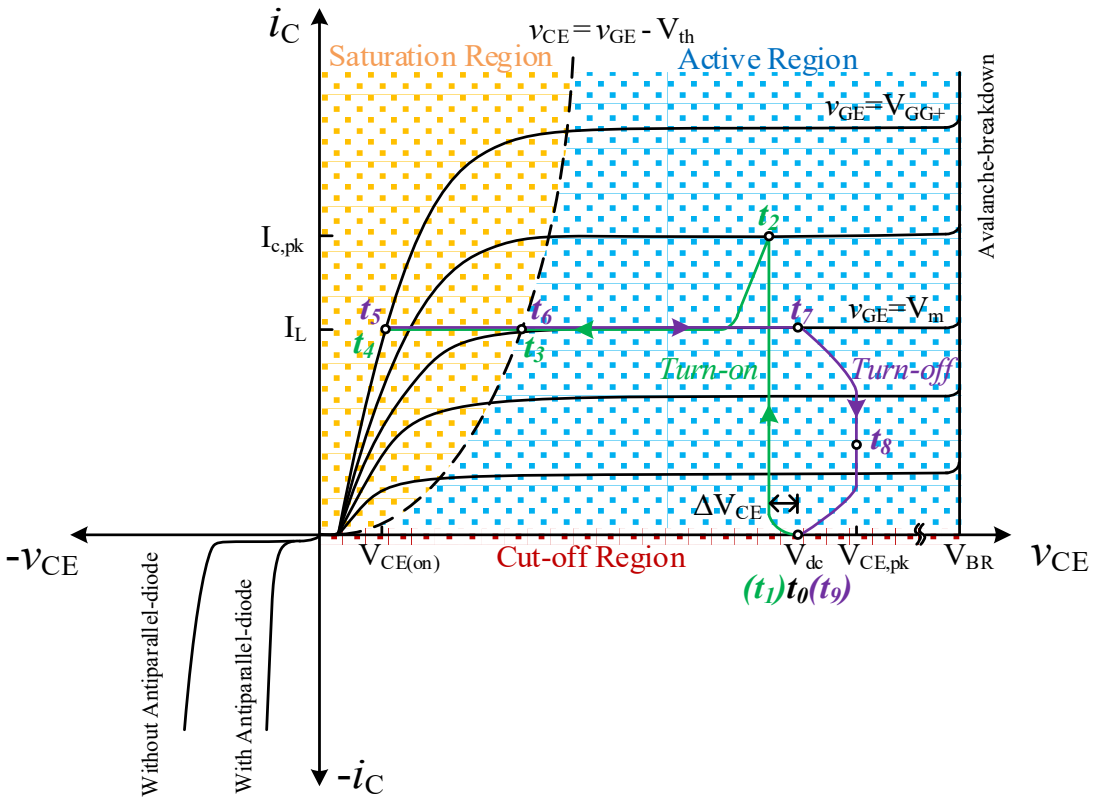


Figure 2-9: Output characteristics of an IGBT device with and without an anti-parallel diode and its switching trajectories.

- Cut-off region ($V_{GE} < V_{th}$)

When a positive V_{CE} is applied across IGBT and the gate-emitter voltage V_{GE} is below the threshold, the IGBT is at off-state with only an extremely small leakage current flowing through the device. However, if the V_{CE} applied across IGBT exceeds the breakdown voltage V_{BR}, the multiplicative current generated during avalanche breakdown can destroy the device as depicted in Figure 2-9.

- Saturation region ($V_{GE} > V_{th}$; $V_{CE} < V_{GE} - V_{th}$)

When the conditions are reached, the operating point of device enters the saturation region which corresponds to the on-state of IGBT. Load current determined by the outer circuit flows through IGBT, at the meantime, a few volts of on-state voltage drop are presented across the collector and emitter terminals. The saturated on-state voltage consists of two portions as represented in Equation (2-4), where the V_{pn} is junction voltage of equivalent transistor and the r is equivalent slope resistance of the curve in saturation region.

$$V_{CE(on)}(T_j, I_C, V_{GE}) = V_{pn}(T_j) + r(T_j, V_{GE}) \times I_C \tag{2-4}$$

It is clear that the on-state voltage is related to the temperature, load current, and gate voltage. The majority of modern IGBT structures have higher $V_{CE\,(on)}$ when the junction temperature rises, which is known as a positive temperature coefficient, excepting the punch-through chip structure.

- Inverse region ($V_{CE} < 0$)

The inverse region is located in the 3rd quadrant of I-V characteristics. Modern asymmetrical type IGBTs, e.g. FS, are best suited for and designed to withstand voltage from collector to emitter, and they have a limited reverse voltage withstand capability. Thus, in most of cases where load current commutation is required, an anti-parallel diode is added to withstand and conduct any transient reverse voltage and current.

- Active region ($V_{GE} \geq V_{th}$; $V_{CE} \geq V_{GE} - V_{th}$)

The operating point only traverses the active region during turn-on and turn-of transients within a short time period, and it is not permissible for IGBT module to be operated in the active region statically due to numerous power losses and severe thermal instability [12]. In the active region, the gate-emitter voltage is linearly proportional to the collector current via the transfer characteristic as illustrated in Figure 2-10. The transconductance g_m is defined as Equation (2-5), and it practically rises in proportion to current and voltage and falls when temperature increases [5].

$$g_m(T_j, I_C, V_{CE}) = \frac{\Delta I_C}{\Delta V_{GE}} \tag{2-5}$$

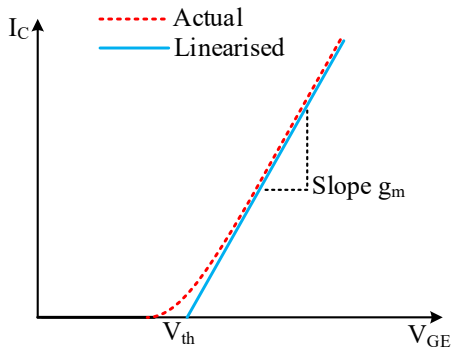


Figure 2-10: IGBT transfer characteristic.

The dynamic trajectories of IGBT operating point during turn-on and turn-off are depicted in Figure 2-9 as well, and the detailed modelling and piece-wise derivation will be done in the next section.

2.4 Dynamic Characteristics

The dynamic characteristics of IGBT module correspond to its overall performance during turn-on and turn-off transitions, which have complex and inconstant transient behaviours that need to be carefully investigated.

2.4.1 Switching Characterisation Modelling

There are many circuit topologies of power converters commonly used in different applications, therefore their associated switching transient characteristics of IGBT

modules need to be investigated. By looking at the most widely used topologies including buck, boost, buck-boost, and half-bridge converters, it is fortunate that a common circuit network is existing among them as highlighted in Figure 2-11. The behaviour of this diode-clamped inductive-load network is the same in all these converters, in other words the switching transient waveforms of IGBT module in this network can represent all application topologies.

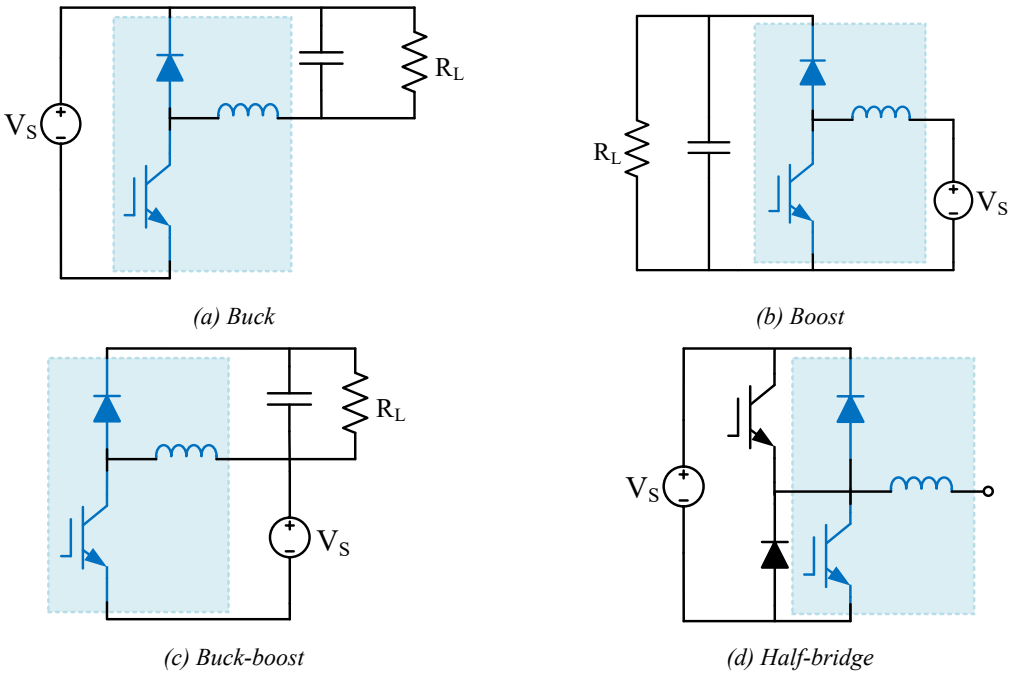


Figure 2-11: Typical power converter topologies with common circuit network highlighted.

Considering the application scenario of high-power IGBT modules in high-speed train, the behaviours of modules in three-phase inverter is going to be discussed deeper. Since the three phase-legs are symmetric, only one phase leg needs to be focused on. As shown in Figure 2-11 (d), one phase-leg has two IGBTs connected in series with a load connection at the midpoint. It has totally eight various transition status as shown in Figure 2-12 and Figure 2-13 for the two different load current directions, respectively. For the Figure 2-12, in the case of load current flowing out of mid-point, the switching commutation can be observed in transitions *T3* and *T4* only. For the Figure 2-13, in the case of load current flowing into the mid-point, the switching commutation can be observed in transitions *T5* and *T6* only.

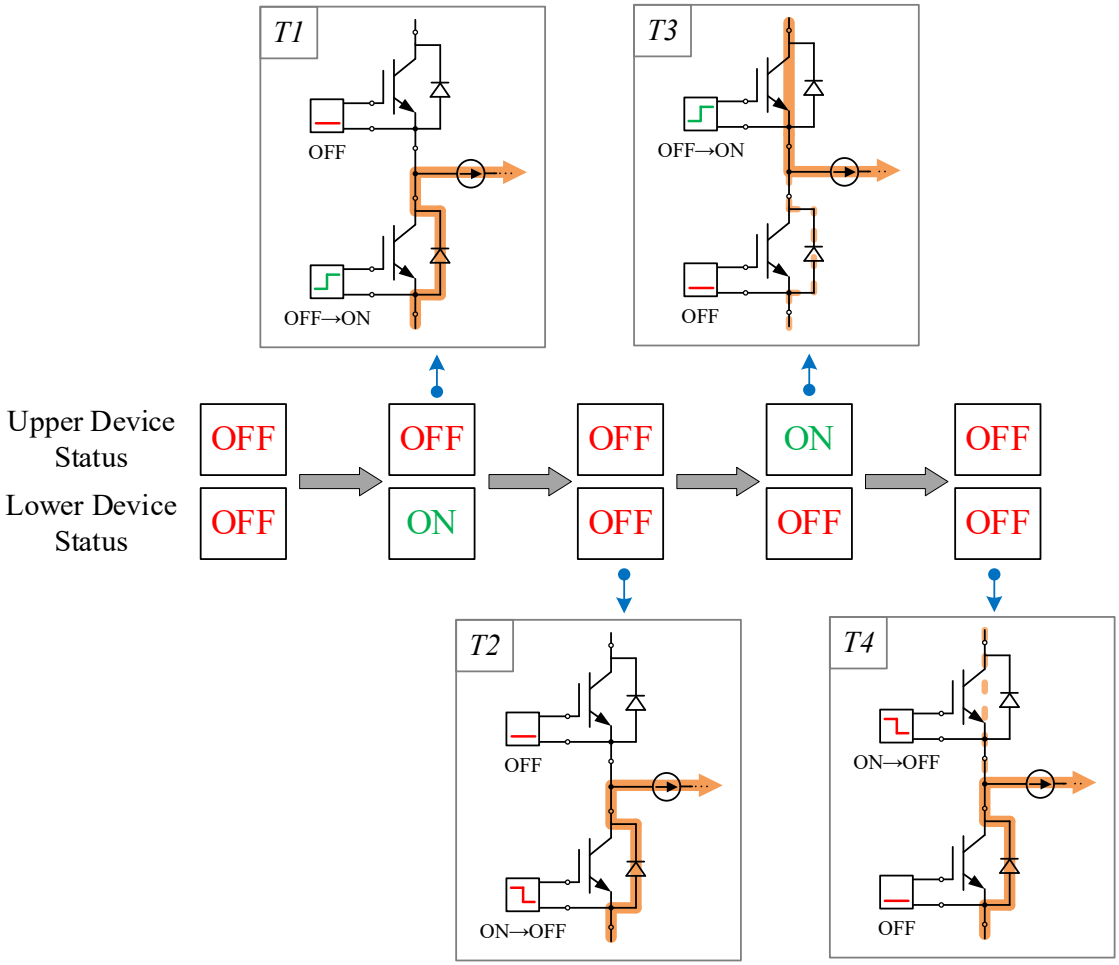


Figure 2-12: Transitions in a bridge leg when the load current is flowing out of mid-point (solid yellow line represents the current flow in the present status, while dashed yellow line represents the previous status).

Therefore, the switching commutation always occurs between the active switch and the complementary FWD, and the diode-clamped inductive-load network can be applied to investigate the dynamic characteristics of high-power IGBT modules in application. It is still true for more complicated topologies applied nowadays in power electronics, including current source converter and three level active-neutral-point-clamped converter and so on [29], with only various parasitics brought by these topologies.

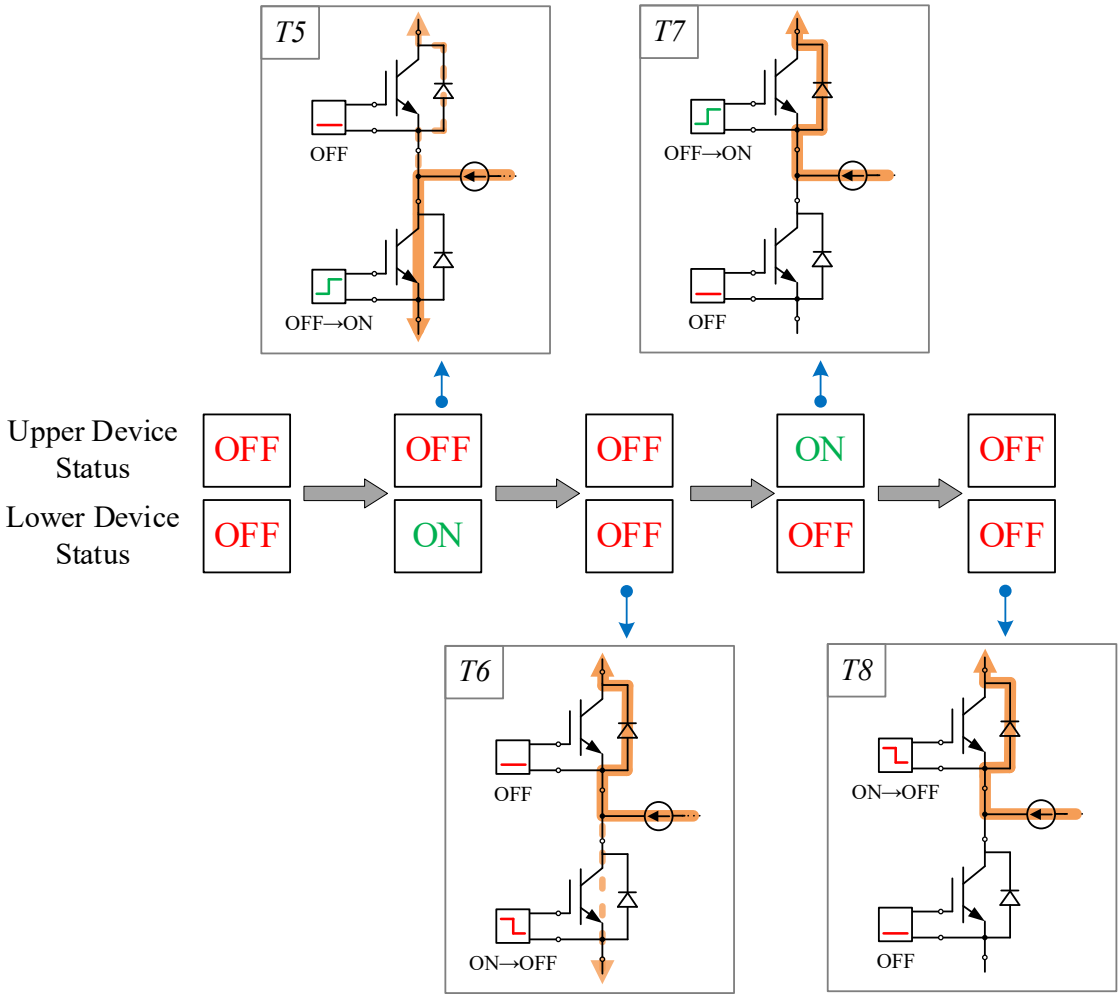


Figure 2-13: Transitions in a bridge leg when the load current is flowing into the mid-point (solid yellow line represents the current flow in the present status, while dashed yellow line represents the previous status).

According to the aforementioned IGBT equivalent circuit and diode-clamped inductive-load network, the circuit model for dynamic characterisation can be established as shown in Figure 2-14.

For the IGBT model, C_{CE} has materially negligible effect on switching waveforms [30], hence it is not included. Only the Miller capacitance C_{GC} is modelled as voltage-dependent due to its large deviation at low and high voltages, which is also proved by the example in Figure 2-3 (b). It can be simplified as two distinctive values of small C_{GC1} and large C_{GC2} when V_{CE} across IGBT is relatively large and small, respectively. Moreover, a voltage-controlled current source is used here to align with the transfer characteristic in the active region.

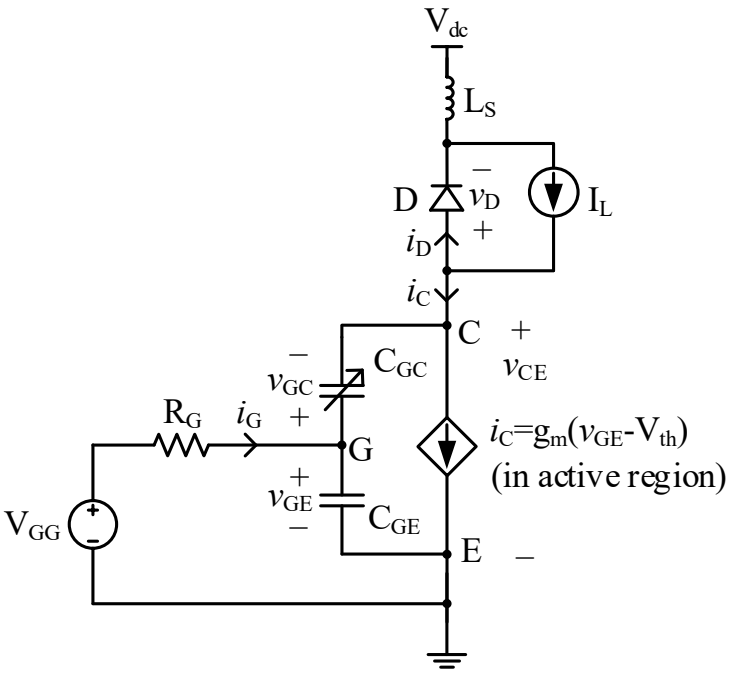


Figure 2-14: Equivalent circuit model for IGBT switching characterisation in hard switching application.

For the common network, the inductive load with high inductance can be modelled to a constant current source. All the parasitic inductance existed in the commutation loop contributed by the DC-link capacitor, the busbar, the device packaging, etc., are lumped into a stray inductance L_S. This lumped inductance features the same behaviour as the distributed parasitic inductance according to circuit analysis.

The gate terminal of IGBT is connected to an external power supply via a gate resistor R_G, which models the conventional gate driver. For simplicity, the parasitic inductance in gate loop is neglected and the internal gate resistor in IGBT module is included into R_G.

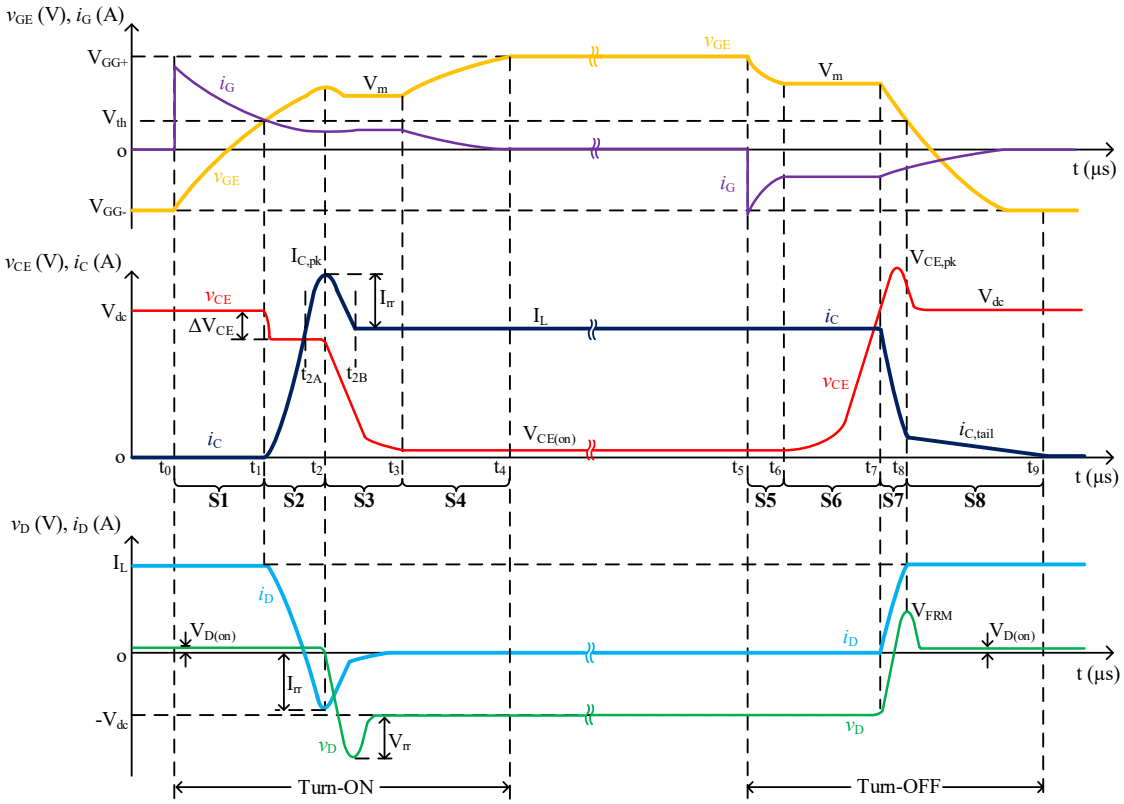
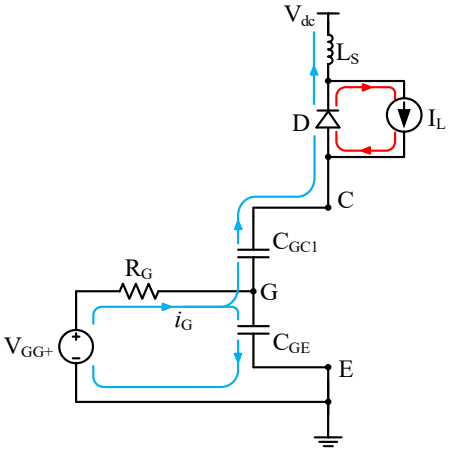


Figure 2-15: Turn-on and turn-off transient waveforms of the IGBT and FWD.

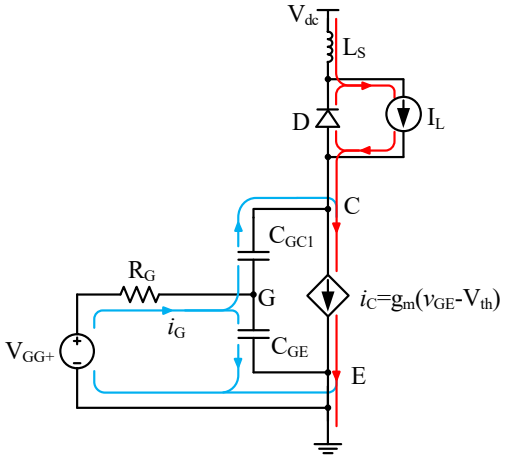
Figure 2-15 shows the full transient switching waveforms of the IGBT and FWD during turn-on and turn-off. The yellow line and purple line show the trajectories of gate-emitter voltage V_{GE} and gate current I_G of IGBT, respectively. The dark blue line and red line represent the trajectories of collector current I_C and collector-emitter voltage V_{CE} of IGBT, respectively. The green line and blue line depict the trajectories of diode voltage V_D and diode current I_D, respectively. The following sections 2.4.2 and 2.4.3 will explain the turn-on and turn-off waveforms in details with help of the piece-wise models in Figure 2-16 and Figure 2-18. Analytical equations describing the transient behaviours will be derived.

2.4.2 Turn-On Transition

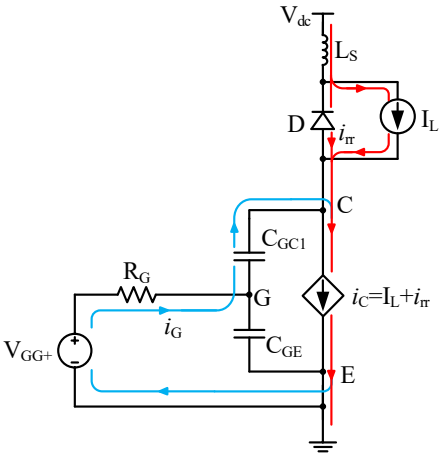
The turn-on switching transients will be discussed following the time sequence, it can be roughly divided into four stages *S1~S4*.



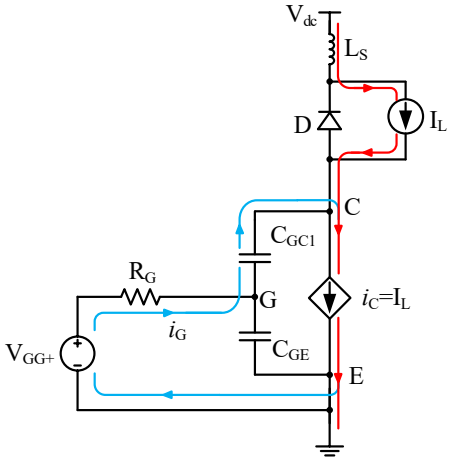
(a) S1 [$t_0 \sim t_1$]: Charging input capacitance



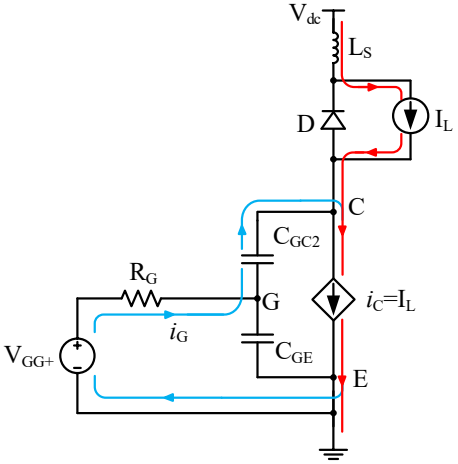
(b) S2 [$t_1 \sim t_2$]: Collector current rise



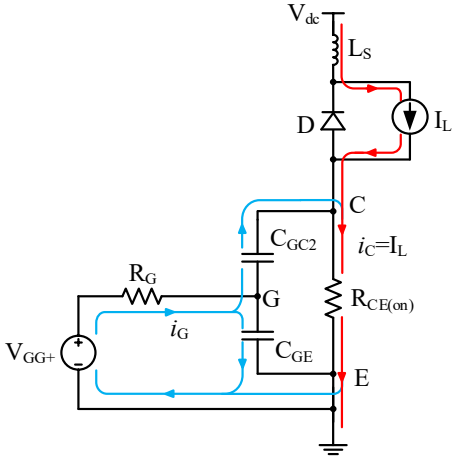
(c) Subinterval [$t_{2A} \sim t_{2B}$]: Current overshoot



(d) S3_a [t2 ~ t3]: Miller plateau; voltage drop



(e) S3_b: C_{GC1} increases to C_{GC2}



(f) S4 [$t_3 \sim t_4$]: IGBT saturation

Figure 2-16: Equivalent circuits and current paths during turn-on at different stages.

➢ Before t_0: Turn-on initial state

At initial state before time t_0 as shown in Figure 2-15, the IGBT is fully switched off, and the conducted current I_C is zero. The collector terminal sustains all the DC bus voltage V_{dc}. At the meantime, I_L is freewheeling through the diode D. To assume a negative gate voltage V_{GG-} is applied to turn off the IGBT, hence at the initial state, the voltage across C_{GE} is fully discharged to negative voltage V_{GG-} provided by gate driver. No current is flowing through the gate at this state as well.

➢ Stage *S1* [$t_0 \sim t_1$]: Turn-on delay

To switch on the IGBT, a positive step gate voltage V_{GG+} is applied at time t_0. The voltage potential difference between V_{GG+} and the initial negative voltage on gate causes the gate current charging the input capacitance C_{GE} and C_{GC} as shown in circuit model Figure 2-16 (a). This gives

$$i_G = i_{GE} + i_{GC1} = (C_{GE} + C_{GC1})\frac{dv_{GE}}{dt} \quad (2\text{-}6)$$

since $i_{GE} = C_{GE}\frac{dv_{GE}}{dt}$ and $i_{GC1} = C_{GC1}\frac{dv_{GC1}}{dt}$, here, the voltage change across C_{GE} is same with C_{GC}, which means $\frac{dv_{GC1}}{dt} = \frac{dv_{GE}}{dt}$, because the voltage potential at collector is fixed at V_{dc} during this stage.

By obeying the Ohm's low, the gate current can be also defined as

$$i_G = \frac{V_{GG+} - v_{GE}}{R_G} \quad (2\text{-}7)$$

The gate current charges the input capacitance and makes V_{GE} to rise from V_{GG-}. To combine Equations (2-6) and (2-7) and integral from time t_0 to t, the function describing the increasing trend of V_{GE} during stage *S1* can be obtained as

$$v_{GE}(t) = V_{GG-} + (V_{GG+} - V_{GG-})(1 - e^{-(t-t_0)/\tau_1}) \quad (2\text{-}8)$$

where $\tau_1 = (C_{GE} + C_{GC1})R_G$ is time constant of the gate charging process at relatively large values of V_{CE}. Equation (2-8) indicates that C_{GE} is being charged from V_{GG-} and its voltage is increasing exponentially.

Based on Equations (2-7) and (2-8), the function describing the decreasing trend of I_G during stage *S1* can be also obtained as

$$i_G(t) = \frac{V_{GG+} - V_{GG-}}{R_G} e^{-(t-t_0)/\tau_1} \quad (2\text{-}9)$$

It is clear that the gate current I_G has maximum value at the beginning t_0, since V_{GE} at this moment is at minimum V_{GG-}, and the voltage difference across R_G is at maximum value. After t_0 the gate current decreases exponentially due to the rising V_{GE}.

In stage *S1*, the IGBT is still at off state, and there will be no current flowing through the IGBT until V_{GE} reaches the threshold V_{th} at time t_1. Hence, the time duration from t_0 to t_1 can be treated as the turn-on delay time, it can be calculated from Equation (2-8).

$$t_d = t_1 - t_0 = R_G\,(C_{GE} + C_{GC1})\ln\left(\frac{V_{GG+} - V_{GG-}}{V_{GG+} - V_{th}}\right) \quad (2\text{-}10)$$

The delay time t_d is the key parameter should be noticed in turn-on stage *S1* because it increases the deadtime and may cause a phase shift and even error in the superordinate system of power electronics converter if the delay is severe.

- Stage *S2* [$t_1 \sim t_2$]: Collector current rise

After time t_1, the input capacitance continues to be charged as same as previous stage *S1*. Similarly, V_{GE} in this stage can be described by

$$v_{GE}(t) = V_{th} + (V_{GG+} - V_{th})(1 - e^{-(t-t_1)/\tau_1}) \quad (2\text{-}11)$$

V_{GE} is continued to increase exponentially starting from V_{th} of IGBT as shown in Figure 2-15. As V_{GE} has exceeded the threshold in stage *S2*, IGBT commences conducting current, and I_C is increasing rapidly from t_1 as shown in Figure 2-15. In other words, the load current starts to commutate from FWD into IGBT as shown in circuit model Figure 2-16 (b). Meanwhile, IGBT enters the active region as shown in the output *I-V* characteristics in Figure 2-9. According to the transfer curve in Figure 2-10, a linearised relationship between V_{GE} and collector current I_C is defined as

$$i_C(t) = g_m(v_{GE}(t) - V_{th}) \quad (2\text{-}12)$$

where g_m is the transconductance.

Hence, by substituting Equation (2-11) into Equation (2-12), the rising I_C can be described.

$$i_C(t) = g_m(V_{GG+} - V_{th})(1 - e^{-(t-t_1)/\tau_1}) \quad (2\text{-}13)$$

Taking derivative of Equation (2-13) gives the slope of I_C, which is

$$\frac{di_C(t)}{dt} = g_m \frac{V_{GG+} - V_{th}}{\tau_1} e^{-(t-t_1)/\tau_1} \quad (2\text{-}14)$$

It is clear that the slope is varying with time. For simplicity and the purpose of obtaining a quantitative I_C slope, the V_{GE} is assumed to be linear during time duration $t_1 \sim t_2$, thus the input capacitance is equivalently charged by an average gate current of this stage. Thereby, the average current slope can be simplified and calculated by Equation (2-15).

$$\frac{di_C}{dt} \cong g_m \frac{V_{GG+} - V_{th} - \frac{I_L}{2g_m}}{R_G(C_{GE} + C_{GC1})} \quad (2\text{-}15)$$

The current rising slope in this stage is vital due to its correlation to current overshoot and switching loss.

Ideally, V_{CE} is clamped at the DC-link voltage as FWD is still conducting current during stage *S2*. However, a drop on the V_{CE} usually appears practically as shown in Figure 2-15, which is related to the induced voltage across the parasitic inductance caused by the rapid current increment, as shown in Equation (2-16).

$$\Delta V_{CE} = L_S \frac{di_C}{dt} \quad (2\text{-}16)$$

In the subinterval $t_{2A} \sim t_{2B}$ as shown in Figure 2-15, the current overshoot appears. After the all the freewheeling current in FWD has commutated into IGBT, the collector current reaches load current I_L at time t_{2A}. I_C continues rising to a peak value because of the reverse recovery character of the complementary FWD. When the diode is turning off from conducting state into the blocking state, the internal stored charge has to be removed, that results in a current flow in the reverse direction in the diode [5]. The reverse recovery current is shown in the diode current waveform I_D in Figure 2-15, which is superposed on I_L resulting a current peak $I_{C,pk}$ in IGBT as shown in the circuit model in Figure 2-16 (c).

Additionally, $I_{C,pk}$ pumps up the V_{GE} a little above the Miller plateau according to the transconductance characteristic in active region.

Figure 2-17 shows the schematic of current in a diode with reverse recovery, and the current is decreasing with a defined speed $di_D/dt = -di_C/dt$.

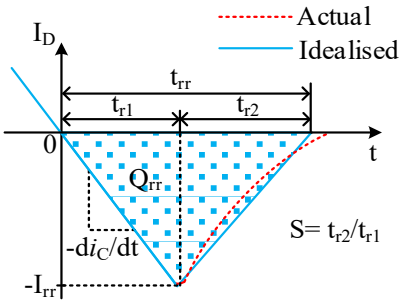


Figure 2-17: Diode reverse recovery and definition of softness factor.

By assuming the reverse recovery trajectory has a triangular shape, the peak reverse recovery current I_{rr} can be calculated by Equation (2-17) [30], where Q_{rr} is the reverse recovery charge, and s is defined as the softness factor which is the ratio between t_{r2} and t_{r1}. The reverse recovery time t_{rr} is the sum of t_{r1} and t_{r2}. If the decay of reverse recovery current is steep, a snappy reverse recovery is given, which can lead to a noticeable induced voltage. If $s > 0.8$, the diode can be treated as having soft reverse recovery [31].

$$I_{rr} = \sqrt{\frac{2Q_{rr}(di_C/dt)}{s+1}} \tag{2-17}$$

Assuming that the diode internal charge recombination can be ignored, thus Q_{rr} equals to the total charge stored in the diode during forward bias, which yields Equation (2-18) [30], where τ_{life} is the carrier lifetime.

$$Q_{rr} = Q_F = \tau_{life} I_L \tag{2-18}$$

Then, to combine Equations (2-17) and (2-18) the peak reverse recovery current can be also represented as

$$I_{rr} = \sqrt{\frac{2\tau_{life} I_L(di_C/dt)}{S+1}} \tag{2-19}$$

From this equation, it can be found that I_{rr} is proportional to di_C/dt and I_L during forward bias. Therefore, the current rising slope during the stage *S2* is significant due to its correlation to turn-on current overshoot. The peak current flowing through the IGBT is not allowed to exceed the safe operating area (SOA) of the device.

- Stage *S3* [$t_2 \sim t_3$]: Collector voltage decay (Miller plateau)

Once I_C achieves peak at t_2 in Figure 2-15, the diode's voltage blocking capability is recovered, thus the collector-emitter voltage V_{CE} starts to decay. As soon as the diode reverse recovery is finished, I_C drops back to the load current I_L and will remain constant. During this stage, the IGBT is still working in the active region, so V_{GE} is clamped at constant based on the transfer curve shown in Figure 2-10. This flat gate-emitter voltage in this duration is called the Miller plateau. From another point of view [32], the Miller plateau is caused by the decline in V_{CE}. A dropping voltage potential at collector terminal results in a displacement current flows through C_{GC} from the gate which needs to be compensated by the whole gate driver output current, hence no current is going to charge the C_{GE} and the V_{GE} is kept at constant. The Miller plateau voltage can be calculated by

$$V_m = V_{th} + \frac{I_L}{g_m} \tag{2-20}$$

As long as V_{GE} is clamped at constant, the gate current keeps at constant as well during this stage, which is

$$i_G(t) = \frac{V_{GG+} - V_m}{R_G} \tag{2-21}$$

Since all the gate current is going to charge the Miller capacitance C_{GC}, as shown in circuit model Figure 2-16 (d), the V_{CE} decreasing slope can be calculated by

$$\frac{dv_{CE}}{dt} = -\frac{dv_{GC}}{dt} = -\frac{i_G}{C_{GC(v_{CE})}} \tag{2-22}$$

In the first portion of this stage, the gate-collector capacitance is at its relatively low value C_{GC1} as V_{CE} is decreasing from a high voltage. However, with the decrease of V_{CE}, C_{GC} is increased significantly when V_{CE} reaches a low voltage as illustrated in Figure 2-3 (b). When V_{CE} declines to the value of V_{GE}, the higher Miller capacitance C_{GC2} is replacing

C_{GC1}, as shown in the circuit model Figure 2-16 (e). That change means the slew rate of V_{CE} will be much slower according to Equation (2-22). The speed change can be seen in the V_{CE} waveform in Figure 2-15 during stage *S3*.

Combining Equations (2-20), (2-21) and (2-22), the function of V_{CE} during this stage can be derived as

$$v_{CE}(t) = (V_{dc} - \Delta V_{dc}) - \frac{V_{GG+} - V_{th} - \frac{I_L}{g_m}}{R_G C_{GC(v_{CE})}}(t - t_2) \qquad (2\text{-}23)$$

And the slope of this reducing voltage can be expressed as

$$\frac{dv_{CE}}{dt} = -\frac{V_{GG+} - V_{th} - \frac{I_L}{g_m}}{R_G C_{GC(v_{CE})}} \qquad (2\text{-}24)$$

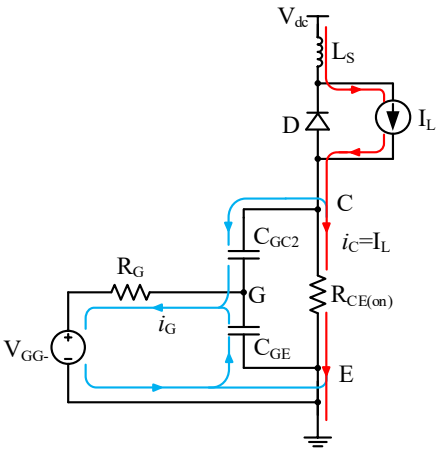
It should be noticed that in this stage *S3*, the current flowing through IGBT is already high (the load current), thus the dropping speed of V_{CE} determines the energy losses generated directly.

- Stage *S4* [$t_3 \sim t_4$]: Gate charging and IGBT saturation

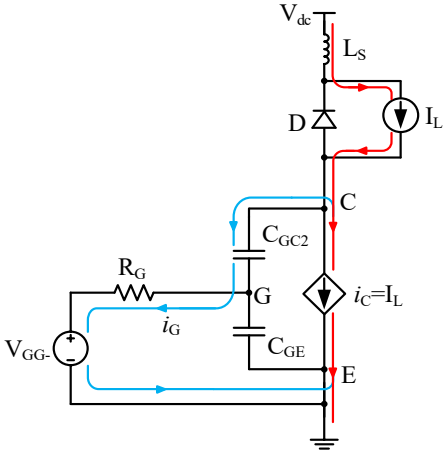
After stage *S3*, the circuit model is shown in Figure 2-16 (f). The operating point enters the saturation area, the gate current starts to charge both C_{GE} and C_{GE}, consequently the V_{GE} increases to the gate voltage V_{GG+}. However, the charging time constant is different with that in stage *S1*, now, $\tau_2 = (C_{GE} + C_{GC2})R_G$. Until V_{CE} gradually drops to the on-state voltage of the IGBT, the whole turn-on transition is completed.

2.4.3 Turn-Off Transition

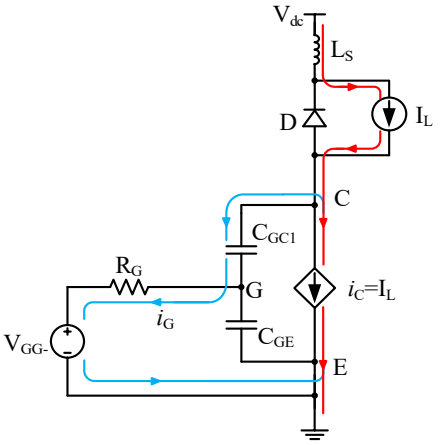
The turn-off switching process is basically reversed transients of turn-on process, except the current tail period and no FWD reverse recovery. It also can be roughly divided into four stages *S5*~*S8*.



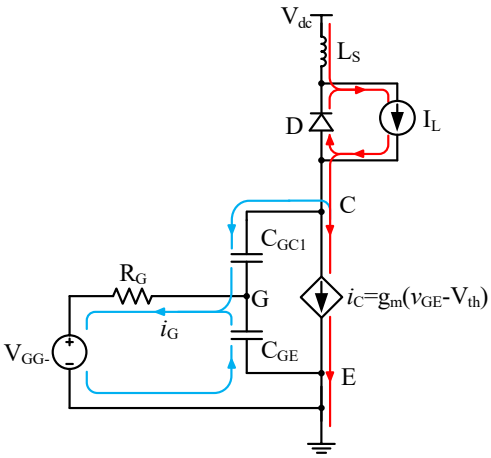
(a) S5 [$t_5 \sim t_6$]: IGBT saturation



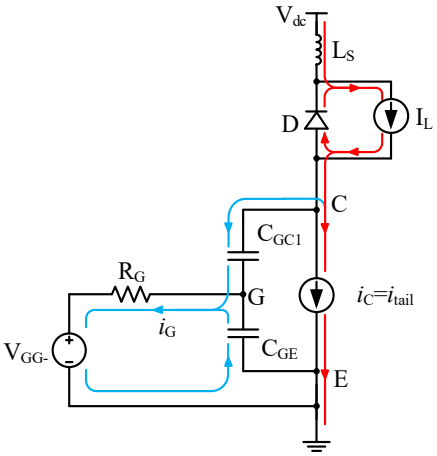
(b) S6_a [$t_6 \sim t_7$]: Miller plateau; voltage rise



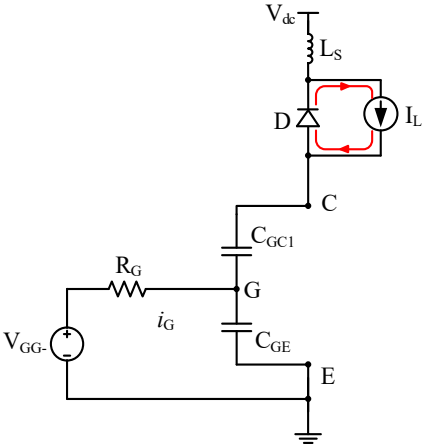
(c) S6_b [$t_6 \sim t_7$]: C_{GC} value decreases to C_{GC1}



(d) S7 [$t_7 \sim t_8$]: Collector current drop



(e) S8 [$t_8 \sim t_9$]: Tail current



(f) After S8: Fully off

Figure 2-18: Equivalent circuits and current paths during turn-off at different stages.

➢ Before t_5: Turn-off initial state

At initial state before time t_5 as shown in Figure 2-15, the IGBT is fully turned-on before commencing the turn-off transition, and it is carrying all the load current I_L. Moreover, a small on-state voltage drop is on the collector-emitter terminals. C_{GE} is fully charged and its voltage is maintained at the positive gate voltage V_{GG+} from gate driver. No current is flowing through the gate at this state as well.

➢ Stage *S5* [$t_5 \sim t_6$]: Turn-off delay

To turn the IGBT off, a negative gate voltage V_{GG-} is applied to discharge the input capacitance C_{GE} and C_{GC} as shown in circuit model Figure 2-18 (a). Consequently, V_{GE} declines from V_{GG+}. Using the similar method, V_{GE} during stage *S5* can be derived as

$$v_{GE}(t) = V_{GG+} - (V_{GG+} - V_{GG-})(1 - e^{-(t-t_5)/\tau_2}) \quad (2\text{-}25)$$

where $\tau_2 = (C_{GE} + C_{GC2})R_G$.

The gate current has the maximum negative value at beginning and then the current drops exponentially toward zero as shown in Figure 2-15, it can be expressed as

$$i_G(t) = -\frac{V_{GG+} - V_{GG-}}{R_G} e^{-(t-t_5)/\tau_2} \quad (2\text{-}26)$$

During this stage, I_C is kept at load current, and V_{CE} increases negligibly from on-state voltage. Hence, it can be seen as a turn-off delay time, which can be calculated by

$$t_d = t_6 - t_5 = R_G(C_{GE} + C_{GC2}) \ln\left(\frac{V_{GG+} - V_{GG-}}{V_m - V_{GG-}}\right) \quad (2\text{-}27)$$

➢ Stage *S6* [$t_6 \sim t_7$]: Collector-emitter voltage increment

After V_{GE} decreases to the Miller plateau voltage, the operating point of the IGBT accesses to the active region, thus the relationship between V_{GE} and I_C should follow the transfer curve. As long as V_{CE} remains beneath the DC-link voltage, the free-wheeling diode is unable to conduct current, therefore the IGBT keeps conducting all I_L. It can be seen in Figure 2-15 that the Miller plateau in V_{GE} appears again, gate current I_G is discharging the Miller capacitance alone. Thus, the gate current also stays at constant,

$$i_G(t) = \frac{V_{GG-} - V_m}{R_G} \quad (2\text{-}28)$$

V_{CE} starts increment, and the change of its capacitance is a reverse process as explained in the stage *S3*. The voltage rises slowly first because of a large C_{GC2}, and followed by a rapid increase when V_{CE} reaches high value as shown in Figure 2-15,

To combine Equations (2-20), (2-22) and (2-28), the function of V_{CE} during this stage can be derived as

$$v_{CE}(t) = V_{CE(on)} + \frac{-V_{GG-} + V_{th} + \frac{I_L}{g_m}}{R_G C_{GC(v_{CE})}}(t - t_6) \quad (2\text{-}29)$$

And the slope of this rising voltage can be expressed as

$$\frac{dv_{CE}}{dt} = \frac{-V_{GG-} + V_{th} + \frac{I_L}{g_m}}{R_G C_{GC(v_{CE})}} \quad (2\text{-}30)$$

- Stage *S7* [$t_7 \sim t_8$]: Collector current drop

Once V_{CE} has increased to the DC-link voltage at t_7, the diode commences forward biasing. Then the current flowing through the IGBT is decreasing and commutating into the diode. V_{GE} is no longer constant and continues discharging again. The IGBT is in active region at this stage, therefore the collector current is corresponding to the transfer characteristic. Equations (2-31), (2-32), and (2-33) can be derived as below.

$$v_{GE}(t) = V_{\mathrm{m}} - (V_{\mathrm{m}} - V_{GG-})(1 - e^{-(t-t_7)/\tau_1}) \quad (2\text{-}31)$$

$$i_C(t) = I_L - g_m(V_m - V_{GG-})(1 - e^{-(t-t_7)/\tau_1}) \quad (2\text{-}32)$$

$$\frac{di_C(t)}{dt} = -g_m \frac{V_{\mathrm{m}} - V_{GG-}}{\tau_1} e^{-(t-t_7)/\tau_1} \quad (2\text{-}33)$$

Similarly, for simplicity and the purpose of obtaining a quantitative I_C slope, the average current slope can be simplified and calculated by

$$\frac{di_C}{dt} \cong g_m \frac{V_{GG-} - V_{th} - \frac{I_L}{2g_m}}{R_G(C_{GE} + C_{GC1})} \quad (2\text{-}34)$$

The steep decline of I_C induces a voltage superposed on the IGBT, so there is a voltage spike in V_{CE} exceeds the bus voltage. Here, di_C/dt has negative value.

$$v_{CE,pk} = V_{DC} + V_{OS} = V_{DC} + L_S \frac{di_C}{dt} \quad (2\text{-}35)$$

➢ Stage *S8* [$t_8 \sim t_9$]: Tail current

During this stage, the collector current has dropped to the tail current level. This tail current is affected by the IGBT manufacture technologies, junction temperature, conducting current and so on, which is unable to be controlled by the gate driver. It leads to a major part of switching losses [17]. Meanwhile, V_{GE} is keeping decrease until it reaches the negative gate voltage V_{GG-} and the turn-off transition is finished.

2.4.4 Switching Losses Modelling

The energy dissipated during switching transients of IGBT module can be estimated by calculating the area of triangular parts of simplified power trajectory as shown in Figure 2-19.

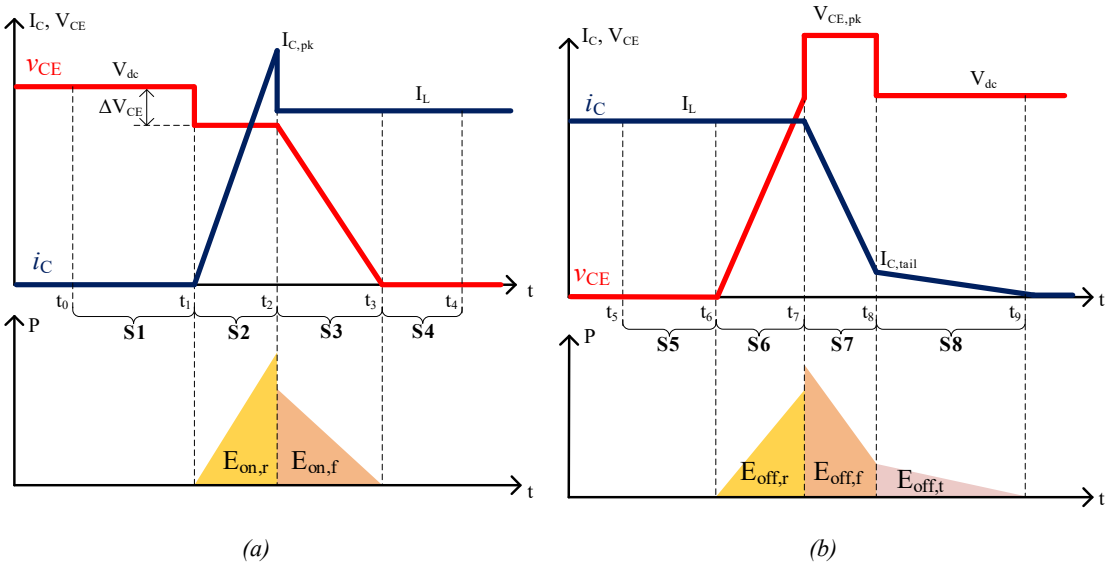


Figure 2-19: Simplified switching losses modelling (a) turn-on transition; (b) turn-off transition.

For turn-on transition, the current overshoot is simplified by assuming the duration between t_2 and t_{2B} in Figure 2-15 is negligible, that means the reverse recovery ceases immediately at t_2. During the current rise stage *S2* of turn-on transition, the energy loss is given by (2-36).

$$E_{on,r} = \frac{1}{2}\frac{I_{C,pk}^2}{\frac{di_C}{dt}}(V_{dc} - L_S\frac{di_C}{dt}) \tag{2-36}$$

Then the energy loss generated during voltage drop stage *S3* is given by (2-37).

$$E_{on,f} = \frac{1}{2}\frac{(V_{dc} - L_S\frac{di_C}{dt})^2}{\frac{dv_{CE}}{dt}}I_L \tag{2-37}$$

Therefore, the total turn-on switching loss can be estimated by (2-38), which is the sum of (2-36) and (2-37).

$$E_{on} = E_{on,r} + E_{on,f} \tag{2-38}$$

For turn-off transition, it is assumed that the voltage overshoot is a constant value of $V_{CE,pk}$ from t_7 to t_8. During the voltage rise stage *S6* of turn-off transition, the energy loss is given by (2-39).

$$E_{off,r} = \frac{1}{2}\frac{{V_{dc}}^2}{\frac{dv_{CE}}{dt}}I_L \tag{2-39}$$

And the energy loss during the current fall stage *S7* can be given as (2-40).

$$E_{off,f} = \frac{1}{2}V_{CE,pk}\frac{I_{C,tail}^2 - I_L^2}{\frac{di_C}{dt}} \tag{2-40}$$

During the current tail stage, the collector current decreases intrinsically from $I_{C,tail}$. The energy loss in this stage can be expressed as (2-41).

$$E_{off,t} = \frac{1}{2}V_{dc}I_{C,tail} \tag{2-41}$$

Therefore, the total turn-off switching loss can be estimated by (2-42), which is the sum of (2-39), (2-40), and (2-41).

$$E_{off} = E_{off,r} + E_{off,f} + E_{off,t} \tag{2-42}$$

It can be easily found that both of turn-on and turn-off switching energy losses are reverse proportional to the collector current and voltage slopes. In other words, a faster switching speed generates lower switching losses during IGBT transients.

2.4.5 Time Definition Criteria

It is important to define the criteria of time intervals to be used for experimental data processing and characteristics extracting. After investigating several industrial manufactures [3, 33-35], the criteria used in the thesis is shown in Figure 2-20.

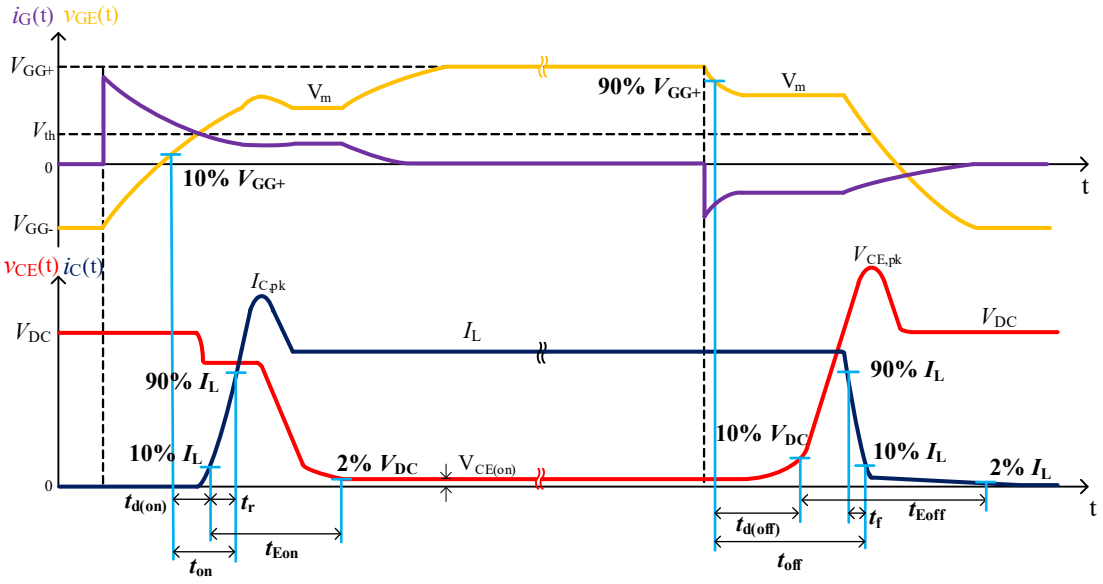


Figure 2-20: Definition criteria of important characteristic parameters.

- Turn-on delay time $t_{d(on)}$

The time duration between V_{GE} reaches 10% of V_{GG+} and I_C rises to 10% of I_L.

- Rise time t_r

The time when I_C increases from 10% to 90% of I_L.

- Turn-on switching time t_{on}

It is the sum of turn-on delay time and rise time.

- Turn-on energy loss calculation time t_{Eon}

The integral time duration between 10% of I_L and 2% of V_{DC} is used.

- Turn-off delay time $t_{d(off)}$

The time interval between V_{GE} arrives 90% of V_{GG+} and V_{CE} rises to 10% of V_{DC}.

- Fall time t_f

The time when I_C decreases from 90% to 10% of I_L.

- Turn-off switching time t_{off}

The time duration between V_{GE} reaches 90% of V_{GG+} and I_C drops to 10% of I_L.

- Turn-off energy loss calculation time t_{Eoff}

The integral time duration between 10% of V_{DC} and 2% of I_L is used.

2.5 Summary of Chapter 2

The physical design and characteristics of high-power IGBT modules are discussed in this chapter. The comprehensive analytical model derived here not only reveals the impact of driving parameters, but also provides the basement for active driving strategies. The switching delay time, current slope di_C/dt, and voltage slope dv_{CE}/dt are all related to the gate resistance R_G and voltage V_{GG} applied on gate driver as concluded in Table 2-3. In addition, the gate current I_G is another driving parameter can be considered. In Figure 2-14, the voltage source V_{GG} in the model can be replaced by a current source I_G. The analytical equations describing the effect of a current source driver can be easily derived and are included in Table 2-3 as well.

Table 2-3 Expressions of key switching characteristics and impact of gate driving parameters

Stage	Voltage Source GD	Current Source GD
Turn-on S1_delay time	$t_d = R_G\,(C_{GE} + C_{GC1})\ln(\frac{V_{GG+} - V_{GG-}}{V_{GG+} - V_{th}})$	$t_d = \frac{(V_{th} - V_{GG-})(C_{GE} + C_{GC1})}{I_G}$
Turn-on S2_i_C rise slope	$\frac{di_C}{dt} \cong g_m \frac{V_{GG+} - V_{th} - \frac{I_L}{2g_m}}{R_G(C_{GE} + C_{GC1})}$	$\frac{di_C}{dt} \cong g_m \frac{I_G}{C_{GE} + C_{GC1}}$
Turn-on S3_v_{CE} drop slope	$\frac{dv_{CE}}{dt} = -\frac{V_{GG+} - V_{th} - \frac{I_L}{g_m}}{R_G C_{GC(v_{CE})}}$	$\frac{dv_{CE}}{dt} = -\frac{I_G}{C_{GC(v_{CE})}}$
Turn-off S5_delay time	$t_d = R_G(C_{GE} + C_{GC2})\ln(\frac{V_{GG+} - V_{GG-}}{V_m - V_{GG-}})$	$t_d = \frac{(V_{GG+} - V_m)(C_{GE} + C_{GC2})}{I_G}$
Turn-off S6_v_{CE} rise slope	$\frac{dv_{CE}}{dt} = \frac{-V_{GG-} + V_{th} + \frac{I_L}{g_m}}{R_G C_{GC(v_{CE})}}$	$\frac{dv_{CE}}{dt} = -\frac{I_G}{C_{GC(v_{CE})}}$
Turn-off S7_i_C drop slope	$\frac{di_C}{dt} \cong g_m \frac{V_{GG-} - V_{th} - \frac{I_L}{2g_m}}{R_G(C_{GE} + C_{GC1})}$	$\frac{di_C}{dt} \cong g_m \frac{I_G}{C_{GE} + C_{GC1}}$

CHAPTER 3

Gate Driver Unit and Development

Gate driver works between the control unit and power device as an interface between digital world and power stage. This chapter introduces the basic outlines and functions of gate drivers for high-power IGBT modules. Moreover, the state-of-the-art active driving techniques are reviewed in this chapter.

3.1 Gate Driver Unit and Conventional Functions

The basic block diagram of gate driver for high-power module is shown in Figure 3-1. It consists of power supply, signal transmission, buffer/amplifier circuit, and protections. Each part will be introduced in the following sections.

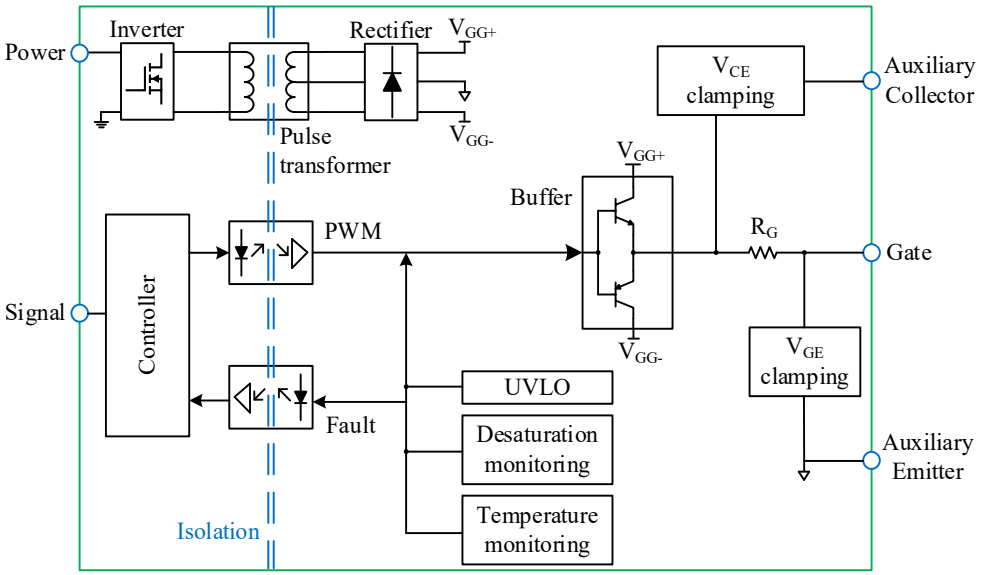


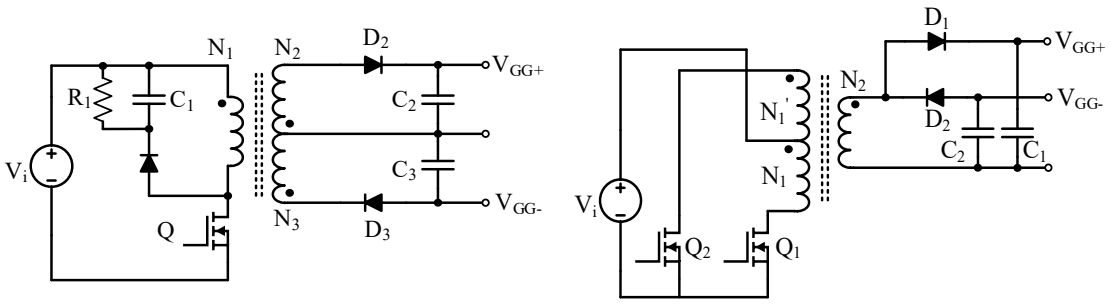
Figure 3-1: Block diagram of conventional gate driver unit for high-power IGBT module.

3.1.1 Power Supply

To turn the IGBT module on and off, a positive voltage V_{GG+} of normally +15V and a negative voltage V_{GG-} up to -15V are required. For high-power modules, these voltages

should be potential isolated and able to provide enough driving energy. Thanks to the IGBT gate structure, the power required in static operation is quite small due to the gate insulator. Hence, the challenge left is the dynamic power demanded during IGBT switching transients from power supply of gate driver. The average gate power required for a certain module can be calculated by (3-1), which is determined by the gate charge of device, the switching frequency, and the voltage values. Additionally, the power dissipated by the driver electronics needs to be considered in power supply design.

$$P_{G,avg} = Q_G f_{sw}(V_{GG+} - V_{GG-}) \tag{3-1}$$



(a) Flyback converter *(b) Push-pull converter*

Figure 3-2: Converter topologies for isolated power supply on gate driver.

The isolated DC/DC converters are commonly used to supply the gate driver for high-power module, and most of them are based on the flyback or push-pull topologies [3] as shown in Figure 3-2.

In flyback converter, the pulsed DC voltage is transmitted to the secondary side of transformer, and the output voltage can be determined by the switch duty cycle and ratio of turns. Multiple outputs can be obtained using an additional winding, diode, and capacitor. The flyback converter is well-suited for transmitting power up to 100 watts [12]. The disadvantage of the flyback is that it needs a continuous conducted load, otherwise the voltage will have unwanted increase due to the energy stored [3].

In push-pull converter, the DC input voltage is converted into AC voltage by using two switches on the primary side of transformer. Further second windings can be added for multi-output realisation. This converter is capable to operate over the whole range of duty cycle. With approaching unity duty cycles, it allows the turns ratio of transformer to be

minimised, reducing the transistor currents. However, this topology is prone to the saturation problem in transformer core because the equity in forward voltage drops and conduction times of transistors cannot be guaranteed. Current-programmed control can be employed to mitigate the saturation [12].

Despite of the galvanic isolation provided by the transformer in DC/DC supply, small coupling capacitor exists between primary and secondary sides. The voltage change on IGBTs causes the common mode current, which might cause side effects on gate driver. Hence, the coupling capacitance should be kept small in driver supply design for error-free operation. In some cases, the common mode transient immunity (CMTI) is given as a vital specification for consideration instead of coupling capacitance.

3.1.2 Signal Transmission

For high-power device gate driver, the bidirectional communication between the main microcontroller and the electronics on the secondary side of gate driver must be realised via signal isolator to separate the grounds. The communicated signals could be the switching command from controller to gated driver or the feedback information from gate driver to controller. Commonly adopted signal isolators are based on optical, inductive or capacitive devices [3].

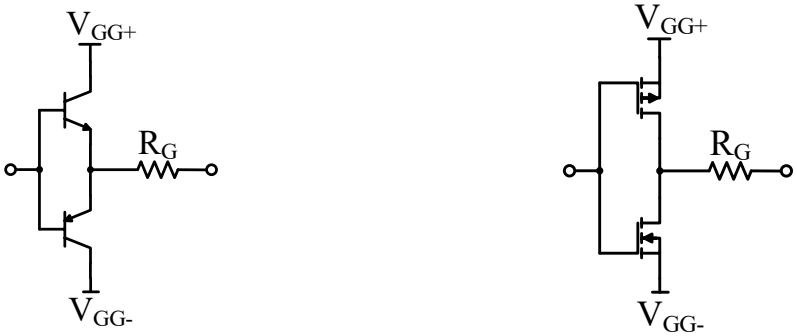
The optocoupler consists of light-emitting and light-sensitive devices. When using the optocoupler, the propagation delay time between input and output need to be considered in the control algorithm. High-speed optocouplers are now available and they can minimise the effect of delay. The aging of these devices might influence long-term service. Fibre optics has big advantages in the virtually unlimited isolation capability and insensitive to EMI, but the price far exceeds other transmission techniques. Delay time of fibre optics is also a factor that needs to be considered. Pulse transformer has good insulation capability and short propagation delay. Sometimes, it is possible to send the signal and power via the same transformer. Capacitors with suitable dielectric strength and capacitance can be used providing isolation. This technique is more applied in gate driver IC.

Table 3-1 Comparison of signal transmission techniques

	Optocoupler	Fibre optics	Pulse transformer
Isolation	Medium	High	High
Signal completeness	High	High	Low
CMTI	High	High	Low
Delay time	Medium	Medium	Low
Cost	Medium	High	Low

3.1.3 Totem-Pole Circuit

The buffer/amplifier stage in gate driver boosts the power level of control signal from microcontroller to charge and discharge the input capacitance of IGBT. Mostly gate drivers used nowadays are based on voltage source and configured in the totem-pole circuit as shown in Figure 3-3. It can be either bipolar junction transistor (BJT)-based or MOSFET-based [36]. The former has non-inverting control logic and no shoot-through current during transition. The latter can achieve higher speed with sacrifice in the cost of MOSFET component and logic inverter. And the shoot-through current can occur when their common gate voltage is in transition.



(a) *(b)*

Figure 3-3: Totem-pole driver circuit with different devices (a) BJT-based; (b) MOSFET-based.

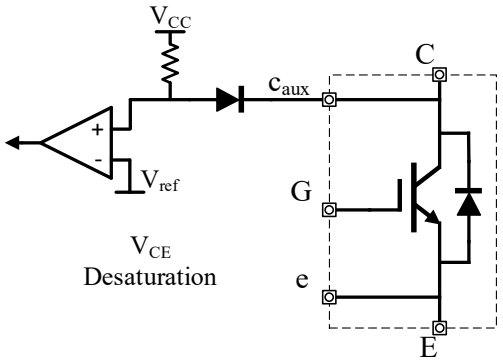
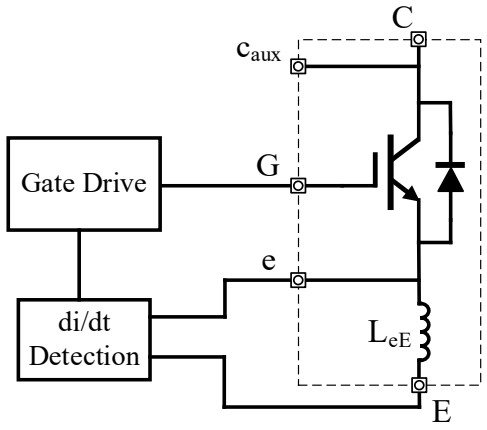
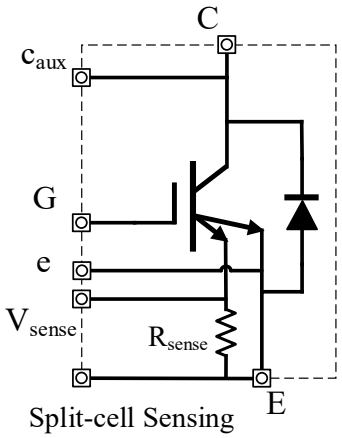
3.1.4 Protective Functions

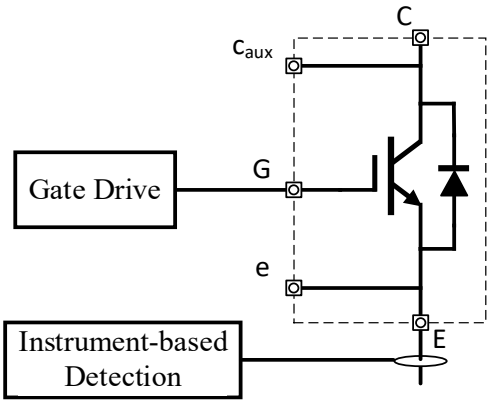
Protective functions are critical to ensure the safety operation of high-power IGBT modules. The common protection objectives include overcurrent, overvoltage, and undervoltage, which will be introduced below.

3.1.4.1 *Overcurrent protection*

Overcurrent is a main factor causing IGBT failure, especially in short-circuit condition. The short-circuit current through IGBT module could be more than 4 times higher than the normal current conducted. Usually, the IGBT module requires to be turned off within 10μs.

Table 3-2 Methods for overcurrent protection

Method	Diagram	Description
V_{CE} desaturation		In the event of short-circuit the IGBT desaturates. V_{CE} rises exceeding the reference value to detect the fault and turn the IGBT off.
di/dt detection		In the event of short-circuit the current induces a voltage across the parasitic inductance on L_{eE} (inductance between power and auxiliary emitter terminals). Comparing the induced voltage with reference to detect the fault.
Split-cell sensing		In some modules with current sensor integrated, it provides the terminals to measure the sensing voltage, which is proportional to the main current in IGBT.

Instrument-based detection		Current measuring instruments such as Hall sensor and Rogowski coil can be implemented to take measurement.

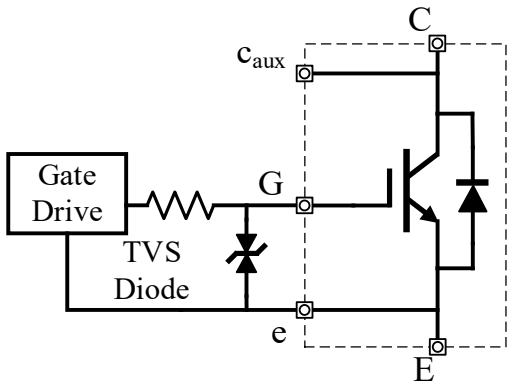
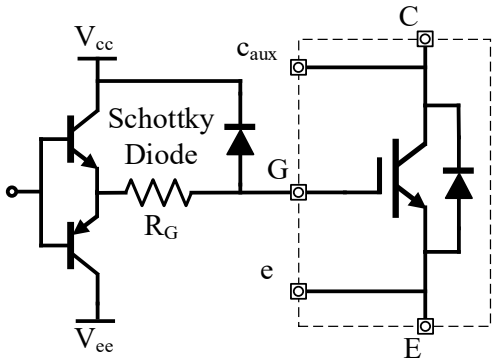
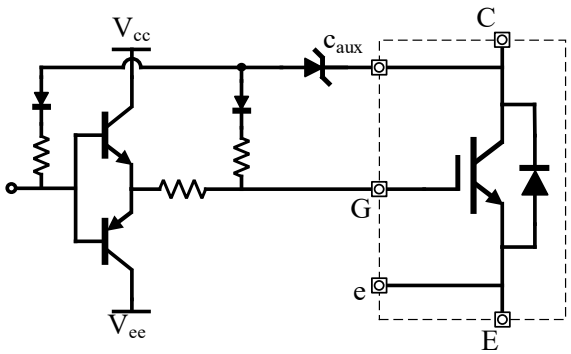
3.1.4.2 *Overvoltage protection*

The voltage at gate terminal of IGBT might increase to the maximum limitation due to the displacement current in Miller capacitor, especially during short-circuit event. Gate voltage should be clamped to avoid gate-oxide breakdown and to limit the maximum short-circuit current. The overvoltage at collector should be avoided by using active clamping circuit.

3.1.4.3 *Undervoltage protection*

For the power supply on gate driver, non-regulated output voltage is sufficient to simplify the control of DC/DC converter, as there is no significant load variation [3]. However, the under-voltage lock-out (UVLO) is required in the case of unexpected voltage decreasing. The undervoltage on gate driver could increase both of switching and conduction losses and might cause overtemperature failure. Monitoring IC can be used on gate driver to detect the supply voltage.

Table 3-3 Methods for overvoltage protection

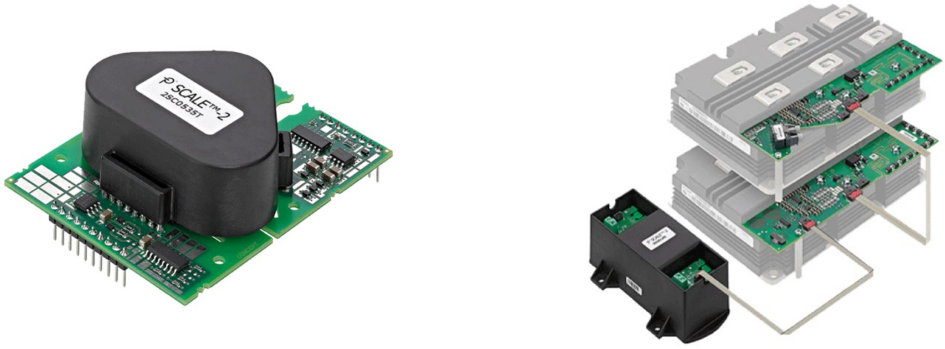
Method	Diagram	Description
TVS diode		It ensures the gate voltage not exceeding maximum.
Schottky diode		Schottky diode can be also used to protect the gate terminal.
Active clamping		As soon as the voltage threshold at collector is exceeded, the transient-voltage-suppression (TVS) diode is conductive, and current injected can turn the IGBT on again to reduce voltage spike.

3.2 Commercial Gate Driver for High-Power IGBT

In the current gate driver market, many power module manufacturers and other power electronics companies have the products ranging from the driver IC for low-power devices to the driver board for up to 1.7kV IGBT modules. However, for the high-voltage modules at 3.3kV, 4.5kV, 6.5kV levels, there are few specialised players, such as Power

Integrations, Amantys, AgileSwitch, Firstack, InPower, etc. The product from Power Integrations and Amantys will be briefly introduced below.

Power Integrations [37] is the gate driver expert for medium- and high-power inverter systems. They deliver high-performance gate driver solutions from 5 kW up to MW for blocking voltages up to 6.5 kV. Its SCALE-2 series gate driver for high-power modules including both of driver core and plug-and-play driver. Driver cores incorporate functions including galvanic isolation, protection functions, DC-DC converter, etc., providing designers with a complete yet extremely flexible system solution. Plug-and-play drivers are ready-to-use and equipped with DC-DC converters, short-circuit protection, active clamping, supply monitoring, soft start and more. SCALE-2 design methodology uses an ASIC chipset to reduce component count and save space.



(a) *(b)*

Figure 3-4: High-power module gate driver from Power Integrations (a) driver core; (b) plug-and-play driver [37].

Figure 3-5 shows the block schematic of driver 1SP0335, which has the following features:

- Power supply monitoring
- Fibre-optic interface (driving input and fault feedback)
- Dynamic V_{CE} monitoring (short-circuit protection)
- Dynamic Advanced Active Clamping DA^2C (overvoltage protection at turn-off)
- Gate monitoring
- Paralleling interfaces ×2 and ×3 for the master-slave connection
- The isolated DC/DC supply ISO5125I is a separate unit not integrated on the driver

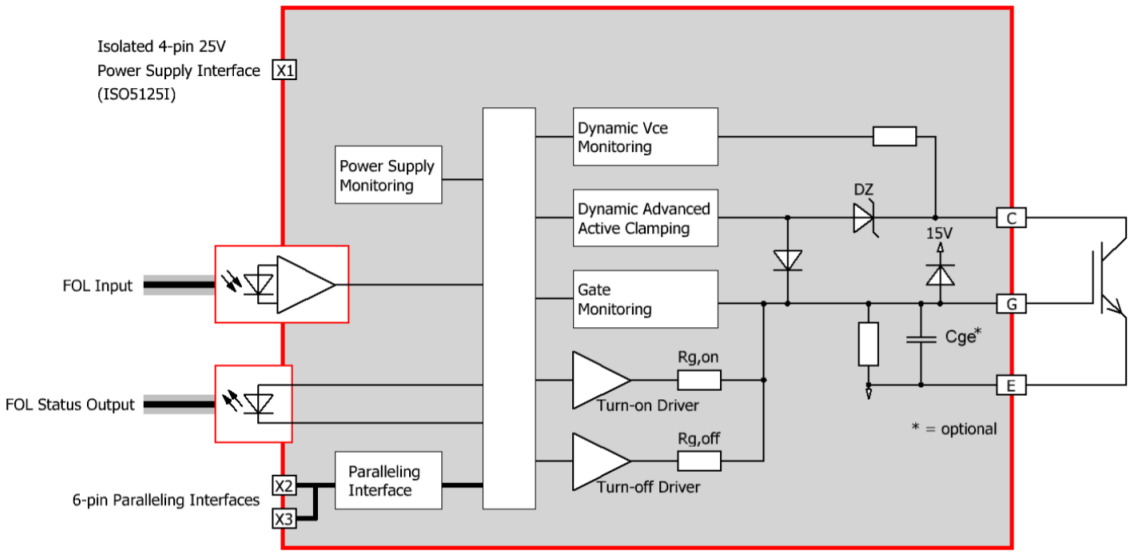


Figure 3-5: Block diagram of Power Integrations driver 1SP0335 [37].

Amantys [38] also designs gate driver for high-power modules up to 6.5kV rating. It has unique feature using Amantys Power Insight technology to communicate with the embedded controller on gate driver over the fibre optic link to extract monitored parameters of the device. This allows the power stack designer to optimise the performance of the stack by configuring and monitoring the gate driver in-situ.

Figure 3-6: Communication feature of Amantys Power Insight technology equipped on gate driver [38].

The specifications of several commercial gate drivers for high-power IGBT modules are compared in Table 3-4.

Table 3-4 Comparison of commercial gate drivers for high-power IGBT modules

Company	Power Integrations	Amantys	AgileSwitch	Firstack
Gate driver	1SP0335x2x1-33	AP33A	HPFM-HPM	1FSD08110
Gate output voltage (V)	+15 / -10	+15 / -8.8	+15 / -10	+15 / -10
Gate output power (W)	3.5	5	7	8
Max. dv/dt (kV/μs)	50	NA	50	NA
UVLO value (V)	+12 / -4.85	+12.9 / NA	+12.8V / NA	+12.7V / NA

3.3 Review of Gate Driving Techniques

Substantial research on enabling the adjustment of current and voltage transient trajectories of power semiconductor devices in hard switching applications have been published. This section gives an overview of these driving concepts, including passive drivers and active drivers, and their pros and cons will be discussed. Figure 3-7 shows the categorised state-of-the-art IGBT driving methods.

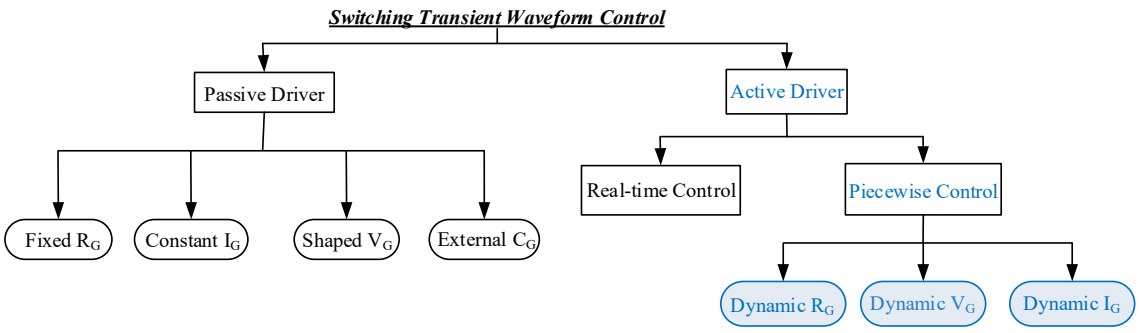
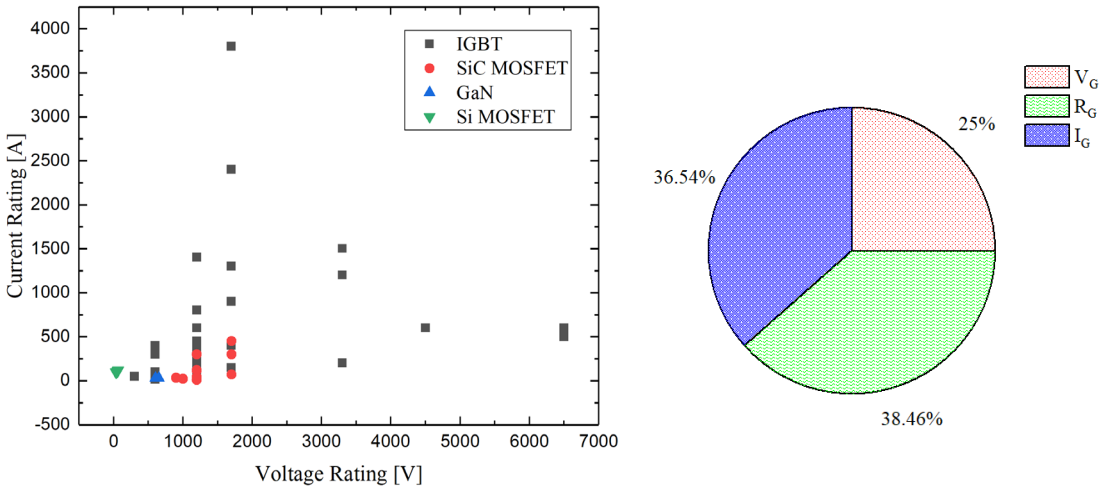


Figure 3-7: Classification of gate driving techniques in switching trajectories control.

The passive driving concepts normally have a predefined driving output, which is unable to adjust during the operation. The CGD is a typical fixed driving concept, which needs the user to pre-set the gate resistance R_G to regulate the switching characteristics of power

device, thus meeting the field application requirements. Small modifications can be applied on the CGD to improve the switching performance, for example, separating the turn-on $R_{G,on}$ and turn-off $R_{G,off}$ through circuit design to meet different turn-on and turn-off requirements. However, they still lack flexibility. The active driving concepts enable the gate driver to dynamically control its output parameter (e.g. R_G) for each characteristic interval within a switching transition. It relies on controlling active components to realise the feature, accompanying with more complicated electronic circuit design.

The research in active driving concept has drawn attention in recent years. A statistic overview of the state-of-the-art research in this field is shown in Figure 3-8. From the device under test (DUT) perspective as shown in Figure 3-8 (a), the majority of research are concentrated on the low- or medium-power devices. However, the active driving concepts for high-power devices are still in a lack of study. From the controlled driving parameter perspective, the conceptual implementation realised by controlling gate voltage V_G, gate resistor R_G, and gate current I_G are almost equivalent quantitatively. A comparative study on these driving parameters is needed.



(a) *(b)*

Figure 3-8: Statistics of 52 research in active gate driving techniques (a) from DUT perspective; (b) from driving parameter perspective.

3.3.1 Passive Driver Concepts

The passive driver has relatively simple circuit structure, at the meanwhile provides good robustness. Furthermore, it is easy to be integrated into driver IC [39] or power module [40]. However, these features of passive gate driver also made them unable to achieve more advanced performance. Typical concepts of passive driver will be introduced below.

3.3.1.1 *Fixed Gate Resistor*

Selecting R_G used on the CGD is a classic and widely used method to adjust IGBT's switching performance, which is also an essential step when designing power converters. Generally speaking, a higher R_G leads to slower and softer switching characteristics and lower EMI level [41]. However, the switching losses will be increased [3, 17]. Figure 3-9 shows a circuit configuration with two specific gate resistors for turn-on and turn-off switching, respectively. Alternatively, diodes can be series-connected with resistors to realise the same function. Thus, the gate driver is able to meet different turn-on and turn-off requirements in application.

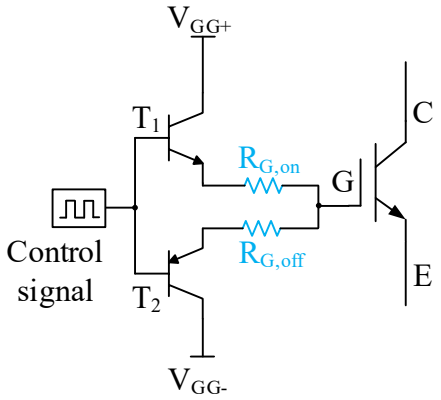


Figure 3-9: Fixed gate resistance driving concept.

3.3.1.2 *Constant Current Source*

Although MOSFET and IGBT are known as voltage-controlled devices, they can be driven by a constant current source as well, as shown in Figure 3-10. Directly injecting current into the gate input terminal could achieve a faster switching speed compared with CGD, hence lowering switching losses. However, the fast-switching results in dramatically high *di/dt*, which causes consequent high current spike during turn-on and high voltage overshoot during turn-off. Other problem caused by the fast-switching is that the ringing during switching become worse, which is reported in paper [42]. An alternative option to limit the turn-on current spike is applying the SiC Schottky diode as the freewheeling diode, due to its negligible reverse recovery effect. The barrier of applying this option is the high cost.

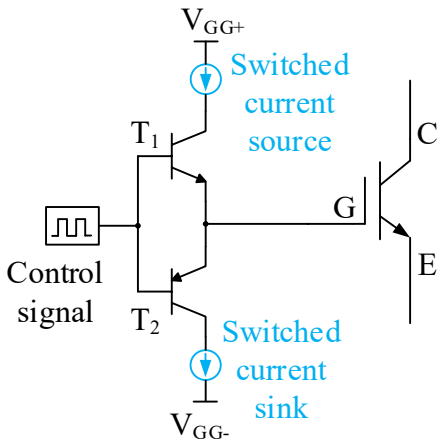


Figure 3-10: Constant current source driving concept.

3.3.1.3 *Shaped Gate Voltage*

As demonstrated in Figure 3-11, the gate driving voltage can be shaped by a designed generator as introduced in paper [43]. When IGBT is being turned on, the upper BJT T_1 is working as an emitter follower, therefore, the emitter voltage is following the output voltage of the generator, which shows a ramping rise. Thus, the IGBT input capacitor is charged by the shaped voltage via R_G. In such a case, R_G can be selected much smaller than the recommended value from IGBT manufactures, and only need to be large enough to prevent oscillations and instability on V_{GE} caused by parasitic inductance and capacitance [43]. By doing so, the rise of V_{GE} is clamped to the shaped voltage ramp, which takes the benefit that collector current *di/dt* is limited, as well as the current spike. Different rising slopes of the ramp voltage can be realised by changing a capacitor designed in the generator. Another advantage of this concept is that the V_{CE} falling edge during turn-on is not controlled by the voltage ramp but R_G, hence the small R_G can accelerate the *dv/dt* stage to reduce the switching loss. However, this method significantly increases the switching delay time due to the slow input capacitor charging at the beginning.

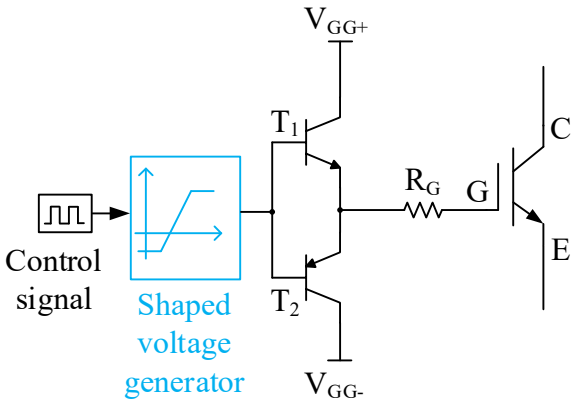


Figure 3-11: Shaped gate voltage driving concept.

3.3.1.4 *External Capacitor*

To achieve both lower overshoot and switching loss of power devices, it is necessary to control *di/dt* and *dv/dt* stages separately due to their dependencies on overshoot and loss. In addition to the shaped gate voltage method above, another simpler method to achieve this is adding an external capacitor C_G across gate and emitter terminals of IGBT as shown in Figure 3-12. For this configuration, *di/dt* stage is set via the sum of parasitic C_{GE} and external C_G, and R_G, while *dv/dt* stage is set via R_G and the Miller capacitor C_{GC}. R_G can be selected smaller comparing with CGD in order to achieve better compromise between overshoot and switching loss. The experimental results in literature [3] shows that, the turn-on loss reduces from 6.4J to 2.8J when adopting this method, while the *di/dt* and current peak are kept same. The drawback of this approach is also obvious that the switching delay time and the gate driver losses are significantly increased due to the increased input capacitance. Additionally, the paper [44] introduced a Zener diode reversely connected to the external capacitor to further improve the turn-off performance.

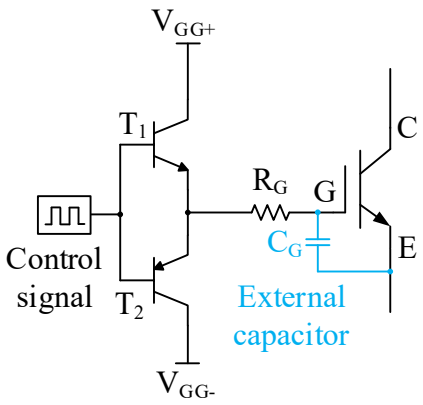


Figure 3-12: External capacitor driving concept.

3.3.2 Piecewise Active Driver Concepts

As shown in the statistic results in Figure 3-8, research proposed to improve the power device's switching transient waveforms by controlling each of the subintervals independently. As aforementioned in Figure 2-15, the turn-on process has been divided into four main parts: *S1* (turn-on delay), *S2* (current rise), *S3* (voltage decay), and *S4* (fully on). Meanwhile, the turn-off process can be divided into four main parts as well: *S5* (turn-off delay), *S6* (voltage rise), *S7* (current decay), and *S8* (tail current). Based on this piecewise principle, the active gate drivers can take specific action for each subinterval. This is a more advanced and flexible technique than the passive drivers.

3.3.2.1 *Active Gate Voltage*

The gate voltages V_{GG+} and V_{GG-} supplied to turn the IGBT on and off can be dynamically changed to control different switching transient intervals as shown in Figure 3-13.

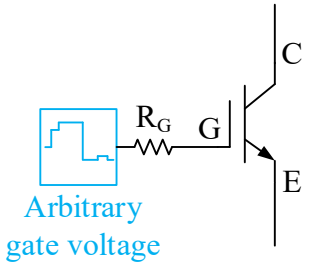


Figure 3-13: Adjustable gate voltage drive.

For turn-on transition, [45] proposed an intermediate voltage method, which has two gate voltage steps. Firstly, the intermediate gate voltage value between the threshold and +15V is set by a voltage divider, and it is applied to turn the IGBT on at *S1* and *S2* stages. This results in the *di/dt* slope under the control of the intermediate voltage value. Then, at the beginning of stage *S3*, the measured I_C information triggers the adjustment of voltage divider, and the driver voltage steps to full +15V to control the rest of turn-on transients. Hence, a better compromise between current peak and turn-on loss can be achieved than CGD. However, this method also makes the larger delay time inevitable. Paper [17] adopts the same control strategy but it is realised by controlling the charging circuit based on a reference voltage, which is set as the desired intermediate voltage value. This method has higher complexity in implementation and control than the previous one. A simpler method to achieve the two-step voltage control can be achieved by adding an additional

voltage source, which is used in papers [3, 46]. They use a voltage higher than the normal +15V to turn the IGBT on during turn-on stages to increase the speed significantly, and then changes back to normal +15V. This method may lead to higher over-current and EMI, and at the risk of gate oxide breakdown in device.

For turn-off transition, an intermediate positive gate voltage less than the threshold is applied in stages *S6* and *S7* in paper [45], which can limit the voltage overshoot effectively. The similar idea can be also found in [47, 48], but they selected using the positive turn-on voltage instead of intermediate one for simplification, which increases the risk of fault turn-on and more energy loss in gate driver. Paper [17] chose to use the reverse steps as explained during its turn-on which applies an intermediate voltage from the beginning of turn-off *S5* and steps to normal turn-off gate voltage in *S6*.

3.3.2.2 *Active Gate Current*

Papers [49-53] apply the circuit topology as shown in Figure 3-14, which has controlled current source and sink added in the driver circuit. For [50, 52, 53], the auxiliary current source is activated to source/sink current, that current is combing with the current of CGD at stage *S2* and *S7* for the sake of controlling *di/dt*. A more accurate control over *di/dt* can be achieved as proposed in [49], since only the controlled current source/sink is working without the CGD at these stages. For this method, the difficulty is to shift from one source to another without any dead time or overlap. In paper [51], the circuit is further improved, in which the CGD has been replaced by another constant current source and sink to achieve more accurate gate current control.

Alternatively, papers [1, 54] use a controlled current source to drive the IGBT, based on the measured feedback signal such as V_{CE} and V_{GE}. The controller uses the information to determine which stage the IGBT switching process is at and then outputs a desired gate current commands for the controlled intervals. However, it requires expensive high-bandwidth electronic components to realise the current source control, measurement, and algorithm.

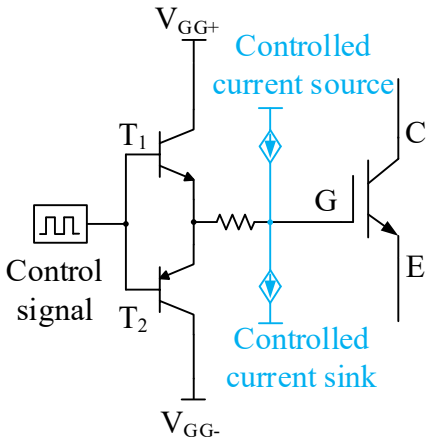


Figure 3-14: Adjustable gate current driving concept.

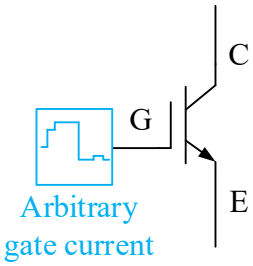


Figure 3-15 Alternative adjustable gate current driver.

3.3.2.3 *Active Gate Resistance*

The active gate resistance driving method is realised in a straightforward way. As shown in Figure 3-16, different gate resistors are installed on the driver circuit board with control switches connected to them. Hence, the gate resistance can be changed by controlling those switches. This method is adopted in some papers [46, 47, 55-60]. More resistors could be added to provide more available resistance values, but the complexity of control signals will be increased as well.

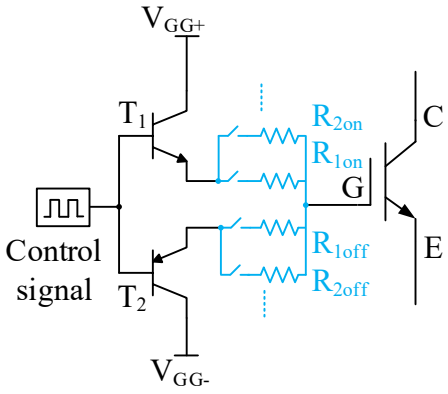


Figure 3-16: Adjustable gate resistance driver.

3.3.3 Real-time Active Driver Concepts

The real-time control is based on closed-loop control method, it can achieve good performance if control parameters are well selected. Papers [61, 62] set desired waveform of collector-emitter voltage as reference signal, and V_{CE} is controlled by the closed-loop controller. The performance is further improved by adding an inner closed-loop controller of *dv/dt* feedback in literature [63]. The *di/dt* slope can also be controlled by the closed-loop controller. The implementation requires complex design and difficult control system design, details can be found in [64-67]. The design process of this driving method is harder than other techniques introduced previously, and the control system stability is also a big challenge due to the nonlinearity of device characteristics. The controller can be implemented either voltage or current driven [68]. High standard for in-situ measuring and feedback circuits are required, thus the cost could increase dramatically. Moreover, the delay effect caused by the parasitic parameters in the driver circuit could greatly challenge the stability of the closed-loop control [51].

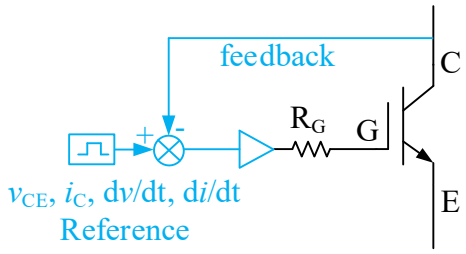


Figure 3-17: Real-time active driver.

3.4 Summary of Chapter 3

The gate driver unit for power semiconductor devices and its functional blocks have been introduced, including its power supply, signal transmission, amplifier, and protective functions, which are essential for gate driver design. Moreover, a review of the state-of-the-art gate driving technology is provided. Comparing with the conventional passive driving methods, the active gate driver is a promising technique which can help to optimise the device switching characteristics and benefit converter systems.

CHAPTER 4

Design of Characterisation Platform

In this chapter, the design of a double pulse test (DPT) system for high-power IGBT modules' switching characterisation will be described. With the increment in power rating of the DUT, the cost for building the test system boosts rapidly due to the expanded test condition range. The main challenge of the design is to achieve both of high testing capability and cost effectiveness. This chapter proposes a comprehensive design procedure to approach the aim during main components selection including capacitor bank and load inductor. Additionally, the auxiliary hardware and the tailored software in the control system and data post-processing are covered. Finally, measurement instruments and skills are discussed for correct and accurate measurement.

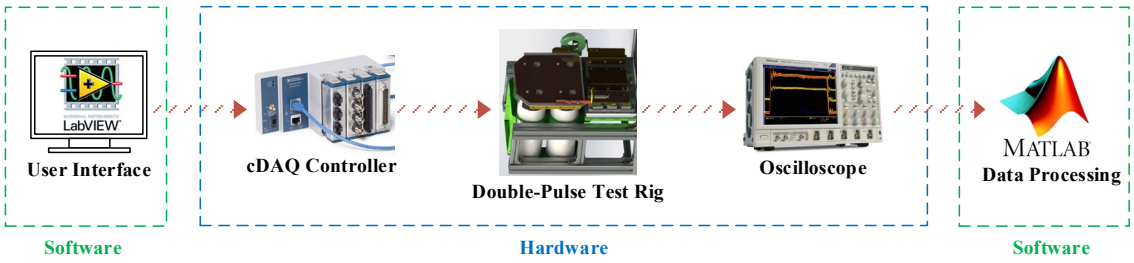


Figure 4-1: Overview of the designed switching characterisation system.

4.1 Principle of Double Pulse Test

To investigate and characterise the transient switching performance of the power semiconductor devices, including the current/voltage transition speed, dynamic overshoots, and switching losses, etc., the DPT is commonly adopted in both industry and academia [29, 69]. It is advantageous that the characteristics of power devices can be obtained without applying them in the real converter application, especially for those medium or high power (e.g. from tens of kilowatt to megawatt level) modules, which has rigorous requirements in terms of feasibility, instrument, and safety concern for

laboratory. A well-designed DPT platform can provide numerous information of the DUT listed below.

- Transient switching characteristics of semiconductor switch and freewheeling diode under a variety of conditions, e.g. load current, load voltage, and junction temperature.
- Behaviours of the gate driver and the impacts on the semiconductor device characteristics caused by adjustment of gate driver's parameters, e.g. gate resistor R_G.
- Static and dynamic current/voltage distribution when several power switches are connected in parallel/series (with few amendments in the interconnection of semiconductor devices).
- Behaviours of power device in short-circuit event and protective shutdown (with some amendments in the test rig configuration).

The circuit schematic of the DPT platform is shown in Figure 4-2. The lower IGBT module of half-bridge is the DUT, which is driven by an external gate driver with two-pulse control signal, hence the DUT turns on and then off twice during the test. The upper IGBT module is kept at off-state by applying the negative gate voltage or short-circuiting the gate-emitter terminals, thus its anti-parallel diode D_2 of the module works as the FWD providing current path when the DUT is off. During the test, the energy required to operate the DUT at desired operating point is all fed by the DC-link capacitor bank C_{bus}. Therefore, charging the C_{bus} needs to be done at the very beginning of the test. A high-voltage DC power supply can be used to charge the C_{bus} after closing the two high-voltage Relay-1 and Relay-2, while Relay-3 is kept off. After the C_{bus} is fully charged to the selected voltage, then Relay-1 and Relay-2 need to be opened to isolate the voltage source from testing circuit. Then, the controller sends out double-pulse signal with regulated pulse width based on the desired operating point for DUT to formally commence the switching sequence. At the meantime, the oscilloscope captures waveforms via probes during the switching process. After two pulses are finished, the DPT is finished and the C_{bus} must be completely discharged by closing Relay-3.

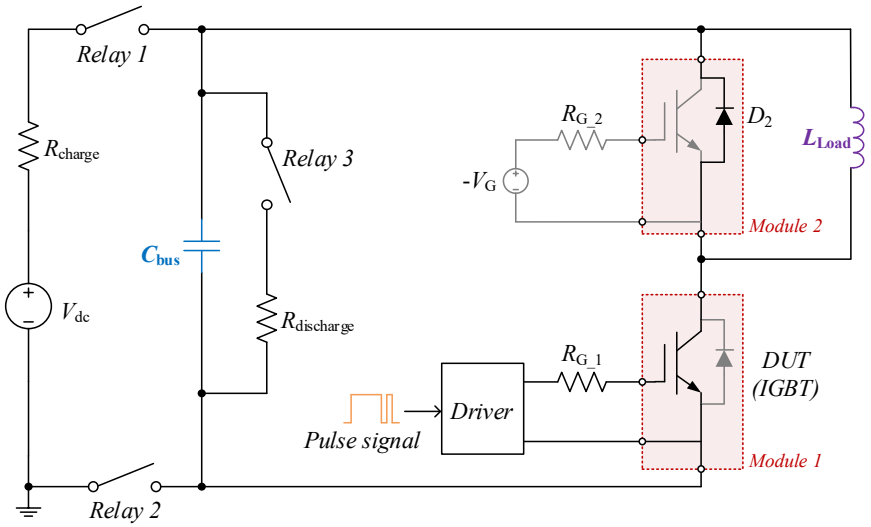


Figure 4-2: Schematic of the double pulse test circuit.

Figure 4-3 depicts the current waveforms of the load inductor I_L, the IGBT (DUT) I_C, and the diode I_D, as well as the voltage waveforms of V_{DC} across the capacitor bank and V_{CE} on the DUT.

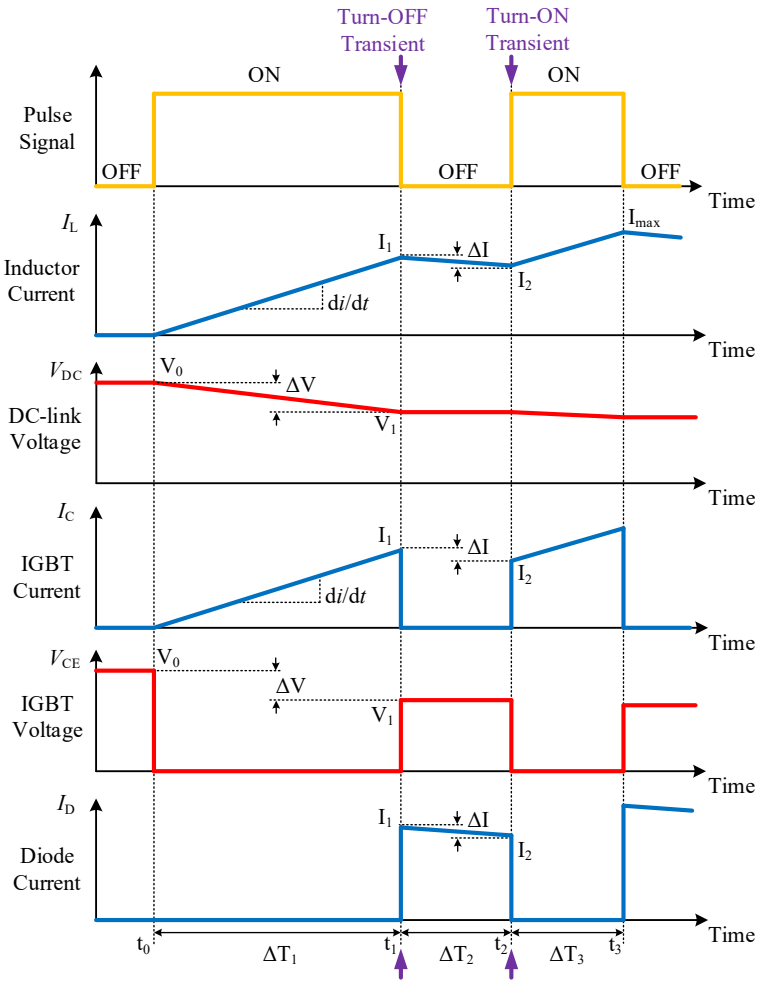


Figure 4-3: Simplified waveforms and timing diagram of a typical double pulse test.

- *Time duration ΔT_1 [$t_0 - t_1$]:*

At the initial time t_0, C_{bus} has been fully charged to a calculated voltage V_0. The DUT is initially off, so that no current flowing through L_{Load}, the IGBT, and the FWD. After t_0, the 1st pulse signal turns IGBT on, then the voltage on C_{bus} is applied across L_{Load} causing an increasing current flow of I_L and I_C. Meanwhile, a portion of energy stored in C_{bus} is transferred into the load inductor and another small portion of energy is dissipated by the stray resistance existed in circuit. Thus, the voltage on C_{bus} decreases during the 1st pulse duration. Since the IGBT is on and conducting current, the V_{CE} across IGBT is almost zero and no current flows in D_2. At the end of duration ΔT_1, I_L and I_C increase to the desired testing current point I_1, meanwhile, V_{DC} decreases to the desired testing voltage point V_1. Hence, the operating condition of I_1&V_1 for investigating the DUT's turn-off switching characteristics under this condition is established at t_1.

- *Time duration ΔT_2 [$t_1 - t_2$]:*

At the time of t_1, the control signal turns the DUT off. After the switching transient finished, the IGBT is at off state, so I_L no longer flows through the DUT and has been commutated to D_2. To consider the dissipation of energy on the diode and stray resistance in circuit, the I_L drops gradually in the duration of ΔT_2 and reaches I_2 at the end of this stage t_2. The voltage V_{CE} applied across DUT is clamped to the bus voltage V_{DC} via the conducted FWD and kept constant at the value of V_1 because no energy extracted from C_{bus}. Hence, the operating condition of I_2&V_1 to investigating the DUT's turn-on switching characteristics under this condition is established at t_2. Obviously, the difference ΔI between I_1 and I_2 should be set as small as possible to provide the same operating condition for the turn-off and turn-on switching transients.

Time duration ΔT_3 [$t_2 - t_3$]:

At the time of t_2, the control signal turns the DUT on again. After the switching transition, I_L continues to increase from I_2 and flows via the DUT. The behaviours of V_{DC}, V_{CE} and I_D are similar to that in duration ΔT_1. At t_3 the IGBT is ultimately turned off, and the I_L will be commutated into diode D_2 for freewheeling and finally decays to zero.

4.2 Wide-Range Testing Realisation

The design process to realise a wide testing range platform with good operating point setting accuracy can follow the proposed flowchart in Figure 4-4. Firstly, the testing range of the designed platform should be determined. Due to more than one mutually constraint factors need to be considered during selection of C_{bus} and L_{Load}, preliminary C_{bus} and L_{Load} can be obtained first. Then, it will be evaluated via a checklist, which has customised coefficient for various restrictions required. If the preliminary selection is satisfied, the platform can be constructed. Otherwise, it needs to be modified and checked again. After that, experimental evaluation is required to validate the error in operating point settings. At some extreme testing conditions, where the accuracy is unacceptable, the calibration in control signal can be processed based on the extracted parasitics.

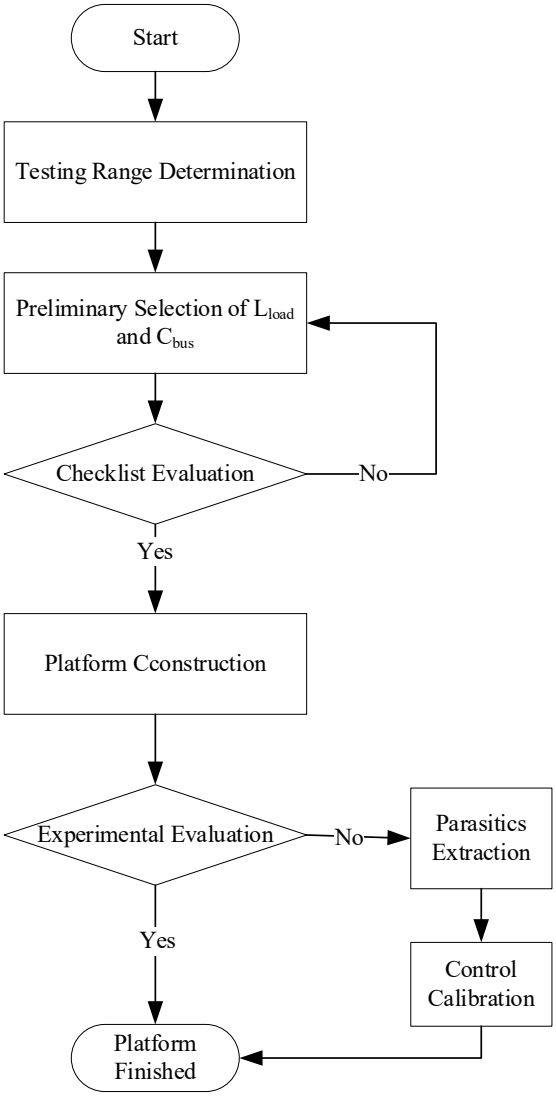


Figure 4-4: Flowchart of the DPT platform components selection and evaluation.

4.2.1 Testing Range Selection

The test platform should cover an operating range as wide as possible under the limitations of the SOA of devices with reasonable constructing difficulty. The voltage overshoot during switching transition must not exceed rated value, hence, the maximum testing voltage can be set to 70% of rated voltage with a 30% safety margin. Since the rated current of IGBT is the maximum continuous current value and the maximum peak current for a short duration usually goes to 2 times of the rated current, it is safe to operate the IGBT up to 100% of rated current. The selection of lower limitations of voltage and current testing range could be relatively unrestricted, but their influences on the requirement of capacitor bank and load inductor should be considered feasibly and economically. Generally speaking, for a built test rig, a lower testing voltage requires a larger capacitor C_{bus} to store enough energy for the DPT, while a lower testing current requires a larger inductor L_{load} to avoid too fast changing in inductor current which increases the error in current switching transients and control difficulty. From the above analysis, the voltage testing range could be set as roughly 20% - 70% of rated voltage, meanwhile the testing current range could be roughly 20% -100% of rated current. Therefore, the expected testing range based on a DUT of 3.3kV/1.5kA ratings can be selected as

- Testing Voltage Range: 500 V ~ 2400 V
- Testing Current Range: 300 A ~ 1500 A

4.2.2 Testing Circuit Modelling

The circuit models for different double pulse test durations can be established for components selection. During ΔT_1 ($t_0 - t_1$), the C_{bus} charges L_{Load}, so the circuit can be modelled as Figure 4-5 (a). The lumped stray resistance R_{S1} models the sum of equivalent on-state resistance of IGBT as well as the equivalent resistance on capacitor bank, load inductor, and busbar conductor. The parasitic inductance of busbar connections can be neglected to compare with the load inductance. During ΔT_2 ($t_1 - t_2$), the load current is freewheeling via the FWD, which can be modelled as Figure 4-5 (b). The stray resistance on the freewheeling loop is lumped as R_{S2}, and the voltage drop on the diode D_2 is

modelled as V_D. In last duration ΔT_3 ($t_2 - t_3$), it is the same manner as duration ΔT_1, hence the circuit model in Figure 4-5 (a) can be used.

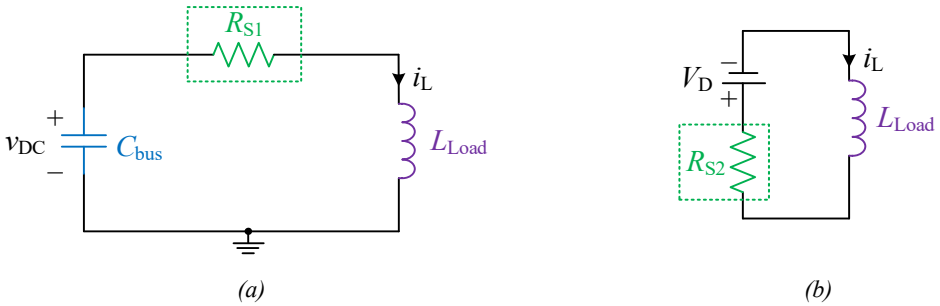


Figure 4-5: Circuit models for different double pulse test durations (a) load inductor charging durations ΔT_1 and ΔT_3; (b) load current freewheeling duration ΔT_2.

As shown in Figure 4-5 (a), the DC-link capacitor C_{bus}, load inductor L_{Load}, and parasitic resistor R_{S1} form a second order RLC circuit. The behaviours of I_L and V_{DC} during the pulse ΔT_1 are equivalent to the natural response of the RLC circuit with the initial conditions of $I_L = 0$ and $V_{DC} = V_0$, which is sketched in Figure 4-6. Since the voltage on capacitor bank will not be discharged to zero during the 1st pulse duration of the DPT, the waveforms of I_L and V_{DC} will stop at somewhere before the time of ¼ resonant period as indicated in the red box in Figure 4-6.

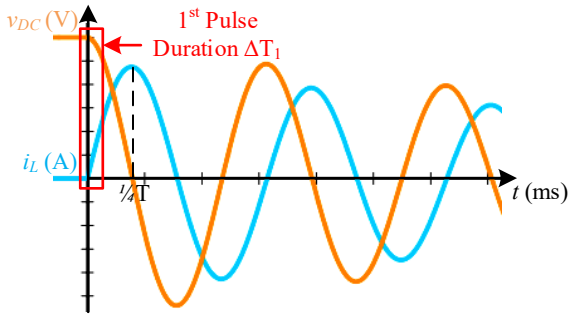


Figure 4-6: Schematic of underdamped natural response of RLC circuit.

Based on the RLC circuit analysis, the current I_L and voltage V_{DC} can be described by equations (4-1) and (4-2). The resonant frequency and period can be calculated by equation (4-3).

$$\frac{d^2 i_L}{dt^2} + \frac{R_{S1}}{L_{Load}} \frac{di_L}{dt} + \frac{1}{L_{Load} C_{bus}} i_L = 0 \qquad (4\text{-}1)$$

$$\frac{d^2v_{DC}}{dt^2} + \frac{R_{S1}}{L_{Load}}\frac{dv_{DC}}{dt} + \frac{1}{L_{Load}C_{bus}}v_{DC} = 0 \quad (4\text{-}2)$$

$$T = \frac{1}{f_0} = 2\pi\sqrt{L_{Load}C_{bus}} \quad (4\text{-}3)$$

This second-order system model complicates both of the components design and control signal calculation because of the nonlinear variations in both of I_L and V_{DC}. Hence, the linearisation can be taken for simplification. However, errors generated by linearisation might lead to unaccepted mismatching between the desired testing point and exact value for the DUT in the DPT. To minimise the error, the worst-case scenario of maximum duration ΔT_{1_max} needed to satisfy the testing range should be kept as small as possible comparing with the ¼ resonant period, which improves the accuracy of linearisation.

The circuit model in Figure 4-5 (a) is simplified to a linear model as shown in Figure 4-7 with two assumptions need to be made. Firstly, the parasitic resistance R_{S1} is neglected to be assumed very small for simplicity. Secondly, the C_{bus} needs to be modelled by a constant DC voltage source with an average value of initial V_0 and final V_1 of duration ΔT_1 as shown in Figure 4-3. Hereby, the expressions for V_0 and V_1 need to be derived in the first place to obtain the V_{avg}.

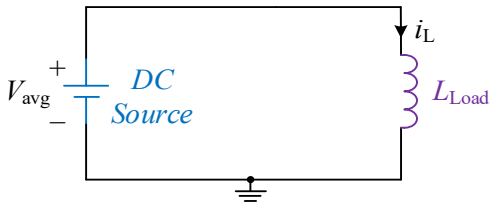


Figure 4-7: Simplified circuit model for the load inductor charging duration ΔT_1.

According to the circuit model of duration ΔT_1 in Figure 4-5 (a) with R_{s1} neglected, all the energy extracted from C_{bus} will be transferred into L_{Load} to derive the Equation (4-4).

$$\frac{1}{2}L_{Load}I_1^2 = \frac{1}{2}C_{bus}(V_0^2 - V_1^2) \quad (4\text{-}4)$$

Therefore, the initial voltage V_0 at time t_0 can be calculated by

$$V_0 = \sqrt{\frac{L_{Load} I_1^2}{C_{bus}} + V_1^2} \tag{4-5}$$

The average voltage of the DC source modelled in Figure 4-7 can be expressed as (4-6).

$$V_{avg} = \frac{V_0 + V_1}{2} = \frac{1}{2}\sqrt{\frac{L_{Load} I_1^2}{C_{bus}} + V_1^2} + \frac{1}{2}V_1 \tag{4-6}$$

To conclude, the model in Figure 4-7 can be used for analysing the first duration ΔT_1, which includes a DC source expressed by Equation (4-6). For the second duration ΔT_2, the circuit model in Figure 4-5 (b) can be applied.

4.2.3 Capacitor and Inductor Selection

The basic principle of DPT is not complicated, however, selecting the proper C_{bus} and L_{Load} to realise wide testing range with restrained funding is challenging due to complicated trade-off existed as concluded in Table 4-1.

It is obvious that if the C_{bus} is very large in Equation (4-5), the voltage drop ΔV can be eliminated to simplify the circuit model. However, forming a capacitor bank with high-voltage capability and large capacitance might cost tremendously. Fortunately, as long as the voltage drop ΔV can be estimated, the desired operating voltage for the DUT can still be obtained at t_1 by estimating the initial voltage V_0. Thus, the required capacitance can be significantly reduced, as well as the cost. Moreover, a reduced capacitance can lower the safety risk when a fault occurs during the test.

Table 4-1 Impacts of DC-link capacitor and load inductor values in the DPT

C_{bus}	**1. *ΔV*** The higher the C_{bus}, the smaller the ΔV is during the time duration ΔT_1. **2. *di_L/dt*** A lower C_{bus} requires a higher initial voltage V_0 to compensate the larger ΔV, which increases the di_L/dt as well. **3. *Cost*** A higher C_{bus} increases the cost significantly as the larger number of capacitors needed. **4. *Safety*** A higher C_{bus} stores more energy at certain voltage, which increases the safety hazard.
L_{Load}	**1. *ΔV*** The higher L_{Load} extracts more energy from C_{bus} to establish certain load current, which causes larger ΔV during ΔT_1. **2. *di_L/dt*** The load inductor current rising speed is determined by the inductance value. **3. *ΔT_1*** The di_L/dt determines the time duration ΔT_1 to establish desired operating current for the DUT. **4. *ΔI*** A higher L_{Load} reduces the current drop during time duration ΔT_2.

As the load current rising speed di_L/dt is related to inductance value as indicated in Equation (4-7), the L_{Load} also determines the time duration of ΔT_1 to establish the operating current for the DUT as shown in Equation (4-8).

$$\frac{di_L}{dt} = \frac{V_{avg}}{L_{Load}} = \frac{\sqrt{\frac{L_{Load}I_1^2}{C_{bus}} + V_1^2} + V_1}{2L_{Load}} \tag{4-7}$$

$$\Delta T_1 = \frac{I_1}{di_L/dt} = \frac{2L_{Load}I_1}{\sqrt{\frac{L_{Load}I_1^2}{C_{bus}} + V_1^2} + V_1} \tag{4-8}$$

Then, during the time duration ΔT_2, the energy stored in L_{load} is dissipated in the freewheeling loop, therefore the inductance value also determines how much the load current will decrease until time t_2. The circuit model for duration ΔT_2 is shown in Figure 4-5 (b), both of the voltage drops on diode and parasitic resistance dissipate the energy stored in the magnetic field of inductor. By analysing the RL circuit model, the variation in load current I_L during ΔT_2 can be expressed as

$$i_L = \left(I_1 + \frac{V_D}{R_{S2}}\right) e^{-\frac{R_{S2}}{L_{Load}}(t-t_1)} - \frac{V_D}{R_{S2}} \quad (t_1 < t < t_2) \tag{4-9}$$

Thus, the current drop during ΔT_2 can be calculated by

$$\Delta I = I_1 - \left(I_1 + \frac{V_D}{R_{S2}}\right) e^{-\frac{R_{S2}}{L_{Load}}\Delta T_1} + \frac{V_D}{R_{S2}} \tag{4-10}$$

It is clear that both of C_{bus} and L_{Load} have several impacts on the performance of the designed test rig. To help with preliminarily determining the range of C_{bus} and L_{Load}, the time durations of ΔT_1, ΔT_2 and ΔT_3 can be considered firstly.

The first duration ΔT_1 should be flexible for various operating points settings, while the durations of ΔT_2 and ΔT_3 can be fixed. The targeted IGBT modules rated up to 3.3kV and 1.5kA normally have a switching time approximately at 1 ~ 2 μs [70, 71]. The durations of the DPT stages should be kept much longer than the device's switching time in order to minimise the influences introduced by IGBT switching transients. The fixed durations ΔT_2 and ΔT_3 can be selected to 50μs. A very large ΔT_2 or ΔT_3 is not recommended because the larger ΔT_2 increases the current drop ΔI during current freewheeling and the larger ΔT_3 increases the largest load current reached at the end of DPT.

ΔT_1 is at minimum when the desired operating point is at max. voltage / min. current of 2400V/300A according to targeted testing range, which means the load charging speed is fastest. By simply assuming no voltage drop during this duration, the V_{avg} is equal to V_1 at 2400V, and the minimum $\Delta T_{1,min}$ is given by

$$\Delta T_{1,min} = \frac{I_{1,min}}{V_{1,max}/L_{Load}} > k_i t_{sw} \tag{4-11}$$

where the device switching time t_{sw} is chosen as 2µs, and the coefficient k_i is chosen to be 10. That means the duration $\Delta T_{1,min}$ is at least 10 times longer than the switching time of the DUT. Hence, the influences introduced by DUT's switching transition process can be reduced. By calculating Equation (4-11), the result shows that the load inductance L_{Load} should be larger than 0.16mH. Considering a margin, it can be preliminarily selected to be 0.3mH. The air-core inductor in preferred to avoid the magnetic saturation.

Then, based on the preliminarily selected L_{Load}, the preliminary C_{bus} can be selected as well. Herein, the voltage drop ΔV during ΔT_1 of whole testing range is desired to be kept much smaller than its corresponding V_1 to give a good accuracy of linearisation without increasing the capacitance too much. From Equation (4-5), this could be expressed as

$$\Delta V_{max} = \sqrt{\frac{L_{Load} I_{1,max}^2}{C_{bus}} + V_{1,min}^2} - V_{1,min} < k_j V_{1,min} \tag{4-12}$$

where the coefficient k_j is chosen to be 1. That means the ΔV_{max} is less than $V_{1,min}$ under the worst-case scenario at the operating point with min. voltage / max. current (500V/1500A). By calculating Equation (4-12), the DC-link capacitor C_{bus} should be larger than 900 µF. To consider the voltage rating of C_{bus} and the commercially available HV capacitors in the market, 4 of 3kV / 300µF film capacitors are preliminarily selected for parallel connection to form a 3kV / 1200µF capacitor bank.

4.2.4 Evaluation and Validation

After the preliminary selection of L_{Load} and C_{bus}, the values need to be evaluated and validated to prove the feasibility or make further optimisation depending on the results. A checklist is proposed as shown in Table 4-2. It is worthy to figure out that this checklist could be generalised for all DPT platform design for any modules at any power ratings, as well as the wide band-gap devices.

Table 4-2 Checklist for evaluation of the capacitor and inductor selection in DPT platform design

Preliminary Selection: $L_{Load} = 0.3\ mH$ $C_{bus} = 1200\ \mu F$ **Test Rig Current Range: $I_{1,max} = 1500\ A$ $I_{1,min} = 300\ A$** **Test Rig Voltage Range: $V_{1,max} = 2400\ V$ $V_{1,min} = 500\ V$** **Fixed Pulse Durations: $\Delta T_2 = 50\ \mu s$ $\Delta T_3 = 50\ \mu s$**		
Duration	**No.**	**Equation and Description**
ΔT_1 (t_0 ~t_1)	**1**	From Equation (4-5) $$V_{0,max} = \sqrt{\frac{L_{Load} I_{1,max}^2}{C_{bus}} + V_{1,max}^2} < V_{rated}$$
		The maximum initial voltage required on C_{bus} must be less than the rating of C_{bus} or DUT. Otherwise, failure will occur.
	2	From Equation (4-8) $$\Delta T_{1,min} = \frac{2 L_{Load} I_{1,min}}{\sqrt{\frac{L_{Load} I_{1,min}^2}{C_{bus}} + V_{1,max}^2} + V_{1,max}} > k_1 t_{sw}$$
		Within the testing range, the minimum ΔT_1 should be larger than the switching time of DUT with a coefficient k_1. In this design, k_1=10. Otherwise, larger error occurs in operating point control.
	3	From Equations (4-3) and (4-8) $$\Delta T_{1,max} = \frac{2 L_{Load} I_{1,max}}{\sqrt{\frac{L_{Load} I_{1,max}^2}{C_{bus}} + V_{1,min}^2} + V_{1,min}} k_2 < \frac{T}{4}$$
		Within the testing range, the maximum ΔT_1 should be smaller than the quarter of resonant period with a coefficient k_2. In this design, k_2=2. Otherwise, larger error occurs in operating point control of low voltage/high current.
ΔT_2 (t_1 ~t_2)	**4**	From Equation (4-10) $$\Delta I_{max} = I_{1,max} - \left(I_{1,max} + \frac{V_D}{R_{S2}}\right) e^{-\frac{R_{S2}}{L_{Load}} \Delta T_2} + \frac{V_D}{R_{S2}} < k_3 I_1$$
		The current drop over this duration should be kept small to compare with operating current with a coefficient k_3. In this

		design, k_3=2%. Otherwise, larger error occurs between turn-on and turn-off switching current values.
ΔT_3 (t_2 ~t_3)	5	From Equation (4-7) $I_{max} \approx I_{1,max} + \Delta T_3 \frac{\sqrt{\frac{L_{Load} I_{1,max}^2}{C_{bus}} + V_{1,max}^2} + V_{1,max}}{2L_{Load}} < I_{rated}$
		The maximum final current reached must be less than the maximum peak current of devices in power loop. Otherwise, failure will occur.

After the designed DPT platform is constructed, the experimental validation of its accuracy in terms of operating point setting for the DUT has been conducted. In Figure 4-8, the error between experimentally measured and the desired operating point over a range of voltage/current tests is presented. The experimental result shows that in most cases the error can be limited within ±5%, which means the designed platform achieves a good accuracy in setting operating conditions for the DUT.

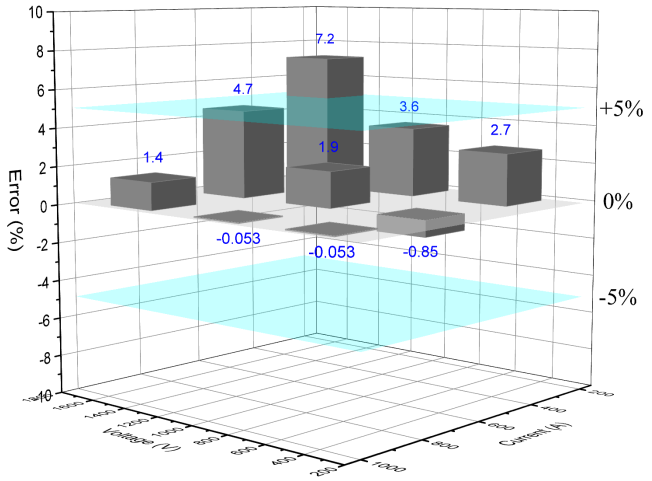


Figure 4-8: Experimental evaluation of errors in operating point setting of designed platform.

When more rigorous accuracy is demanded, measures can be taken including: adjusting the coefficients in the checklist; taking the parasitic resistance *R*s1 into account in the model; using the second-order equations to achieve best accuracy but increases the complexity.

4.3 Auxiliary Hardware Design

Some auxiliary hardware assembled on the design test platform are discussed in this section, including the laminated busbar, the relay board, and the heat-plates.

4.3.1 Laminated Busbar

The laminated busbar is preferred in power converter design to connect the DC-link capacitors and power devices due to its low parasitic inductance. By placing two copper plates in a laminated layer structure, the magnetic fields generated by the current conducted in the plates with opposite direction could cancel each other to reduce the inductance as shown in Figure 4-9.

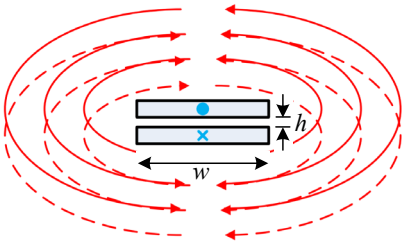


Figure 4-9: Magnetic field overlap caused by paralleled plates.

The parasitic inductance can be estimated by Equation (4-13) according to [72]. Increasing the width w of plates or decreasing the gap h between plates can reduce the parasitic inductance induced. The designed laminated busbar is displayed in Figure 4-10.

$$L \approx \mu \frac{h}{w} \tag{4-13}$$

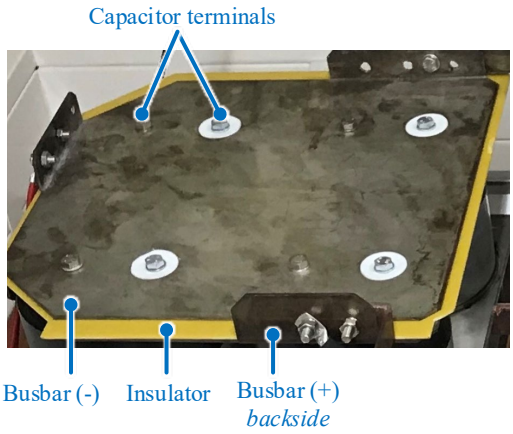


Figure 4-10: Photo of designed laminated busbar.

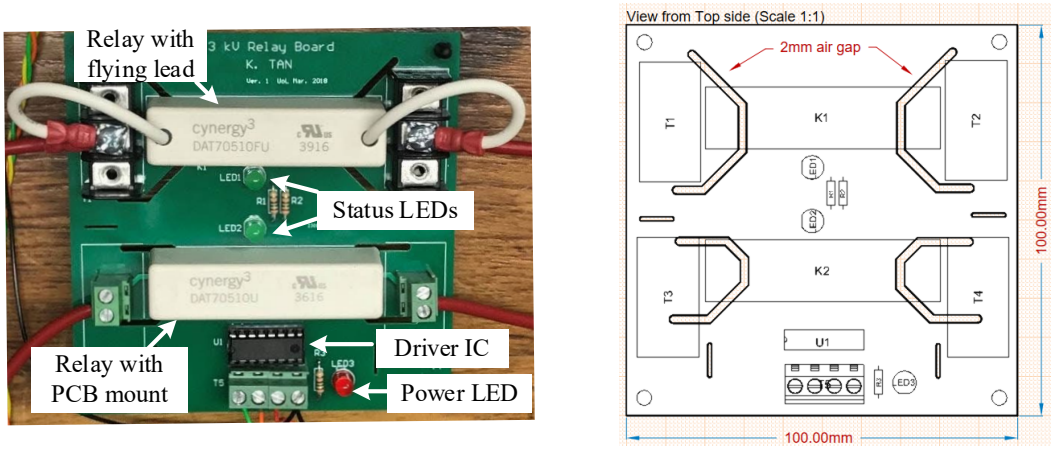
4.3.2 Relay Board for Test Rig

Relay-1 shown in Figure 4-2 are used to connect or disconnect the DC voltage supply to the capacitor bank, while Relay-2 is utilised to isolate the ground of DC supply from test circuit. Since some non-isolated probes might be connected into test circuit for measurement purpose, the ground of oscilloscope will be introduced at the Kelvin emitter of IGBT Module 1 in Figure 4-2. The parasitic inductance between the ground of oscilloscope and the ground of DC supply might cause oscillation in measurement [73], therefore, Relay-2 is introduced and will be opened during the DPT to improve the cleanliness of measurement. The Relay-3 is used to discharge the capacitor bank C_{bus} after the DPT is finished.

Relays with essential high voltage blocking and switching capabilities need to be applied in this design. Additionally, considering the large space required by the HV-IGBT modules and capacitor bank, a space-saving solution for these relays is preferred. The DAT70510U reed relay [74] from Cynergy3 Company has been chosen, which is a printed circuit board (PCB)-mounted relay with small size of 60mm*15.8mm*18.5mm. It has 10kV isolation across contacts, and it is capable to switch maximum 7kV voltage and 2A DC current. This DAT70510U relay can be controlled by 5V coil. Normally, the microcontroller only can supply tens of mA current [75], therefore, a transistor-based ULN2803 driver IC [76] with eight 500mA Darlington pairs are used to amplify the control signal. Two PCB relay boards with two high voltage relays on each are assembled as shown in Figure 4-11 (a). Considering that Relay 1 sees larger voltage difference on its terminals than Relay 2, the flying lead is selected to enhance the insulation. Moreover, 2mm airgap is designed on PCB to further enhance the insulation as shown in Figure 4-11 (b), and the gap distance is chosen based on the Paschen curve in [77]. Light-emitting diodes (LEDs) have been added on relay board to indicate the ON/OFF status of relays and power supply for safety and convenience concerns.

The energy stored in capacitor bank will be dissipated by the discharging resistor. An aluminium housed 6.8kΩ resistor mounted on heatsink with 100W power rating has been selected to ensure the safety. The time constant of the discharging circuit loop is about 8 seconds, thus it takes roughly 1 minute to fully discharge the capacitor bank, which is

acceptable. The experimental result in Figure 4-12 shows the temperature only rises 5°C after fully discharged the capacitor bank with 2kV initial voltage.



(a) *(b)*

Figure 4-11: Designed high-voltage relay board (a) Photograph; (b) Mechanical Schematic.

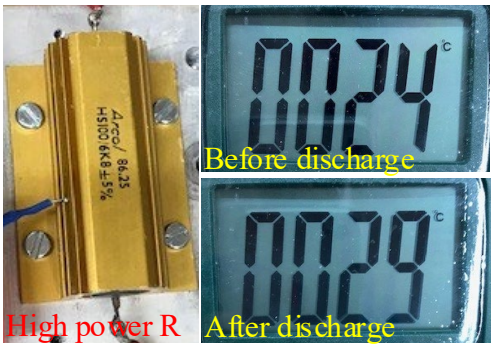


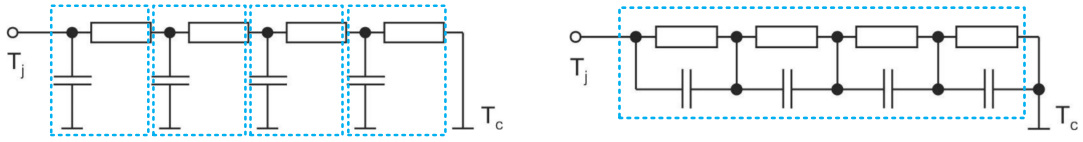
Figure 4-12: The discharging resistor and its case temperature change caused by discharging capacitor bank from 2kV initial voltage.

4.3.3 Heat-Plate and Heatsink Consideration

Two individual heat-plates are assembled beneath the modules to set their operating temperature separately. Hereby, the DUT and the FWD can operate at different temperatures to expand the testing flexibility. However, it is still worth to discuss the necessity of heatsink during the DPT. Literature states that the WBG device's junction temperature rise during DPT is negligibly small [69]. However, considering the higher power handed in this project, an estimation including both of switching and conducting losses during the test is needed.

The Cauer model and Foster model shown in Figure 4-13 are commonly used to describe the thermal behaviour of semiconductor components. The Cauer model reflects the

physical layer setup of the device based on the thermal capacitance and thermal resistance RC elements, while the Foster model has no physical significance but normally used in the datasheet due to the ease of parameter extraction [78].



(a) *(b)*

Figure 4-13: Thermal network (a) Cauer model; (b) Foster model.

As the junction temperature is cared rather than the temperature of each component layer, the Foster model will be used for estimation. The 3300V/1500A module FZ1500R33HE3 is taken as the example. The transient thermal junction-case impedance against power pulse duration is given in module's datasheet. According to the parameters of r_i and τ_i given and Equation (4-14), the transient thermal impedance curve can be extended to a shorter time duration as shown in Figure 4-14.

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} r_i[1 - e^{-t/\tau_i}] \qquad (4\text{-}14)$$

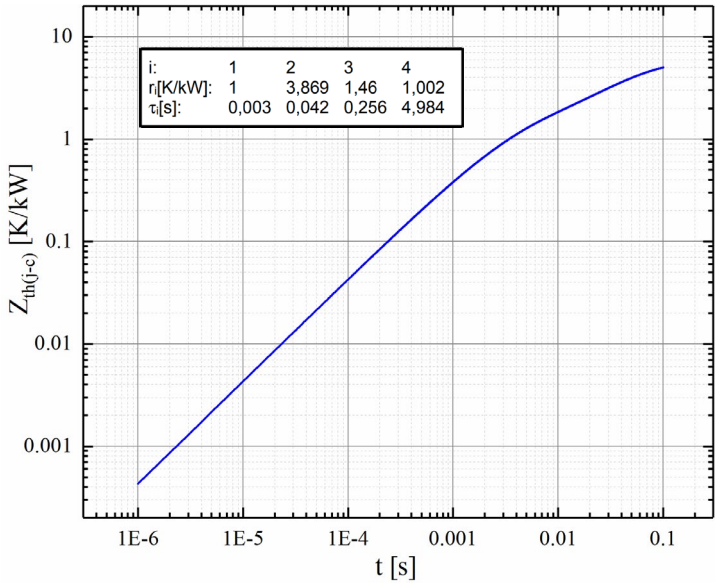


Figure 4-14: Recalculated transient thermal impedance against pulse duration ranging from 1μs to 0.1s.

Assuming a DPT at 1800V/1500A testing point with 500μs conduction time and 1μs turn-on and turn-off switching time during the testing process, the thermal impedance for

conducting and switching duration can be read from Figure 4-14 as 0.2K/kW and 0.0003K/kW respectively. By applying superposition method [79] for each duration, it can be estimated that the junction temperature of IGBT increases only 2.5°C for the whole DPT process. Therefore, the temperature rise of IGBT during the DPT has negligible impact on device performance and the use of heatsink can be ignored. The customised heat-plates are placed directly under IGBT modules as shown in Figure 4-15. The heat-plate has a temperature sensor, so the controller can be accurately controlled. The heat-plate is capable to cover the maximum temperature rating of the Si and WBG devices.

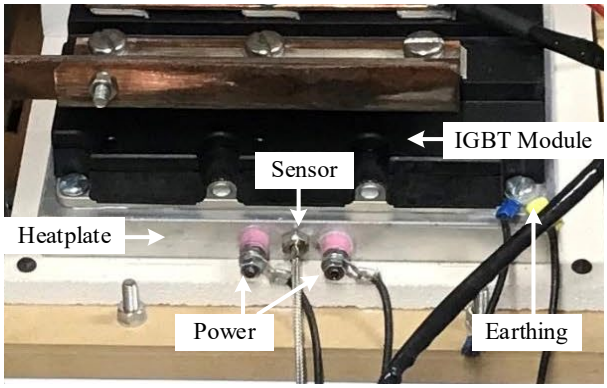


Figure 4-15: Photo of customised heat-plate mounted beneath the IGBT module.

4.4 Computer-Aided Software Design

It is certain that the designed platform will conduct the DPT under a large number of various operating conditions for the DUT, and the double-pulse signal needs to be tailored in pulse width for each test condition. Moreover, a plenty of waveform data is accompanied with the increasing number of tests. Therefore, utilising computer software to accelerate and simplify the DPT procedures is crucial. In this section, a LabVIEW-based user interface for platform control and a MATLAB-based data post-processing tool are proposed.

4.4.1 Control and User Interface

The cDAQ platform built by National Instruments company integrates hardware for data I/O with LabVIEW software to enable engineers implementing system automation. In the designed platform, a cDAQ chassis embedded with a NI-9401 digital module is applied to configure a 5V digital I/O interface to control the relays and gate driver for the DPT.

In LabVIEW, virtual instruments can be configured in the front panel as user interface. In the back-end, the Virtual Instrument Software Architecture (VISA) manages the communication between LabVIEW and cDAQ hardware [80]. The graphical programming used in LabVIEW allows programmers to build programs by dragging and dropping virtual representations of lab equipment and functional blocks. Moreover, it is an inherently concurrent language and suitable for multiple tasks that are performed in parallel. This is a great advantage for test system automation, where it is common practice to execute processes like hardware interfacing, test sequencing, and data recording in parallel.

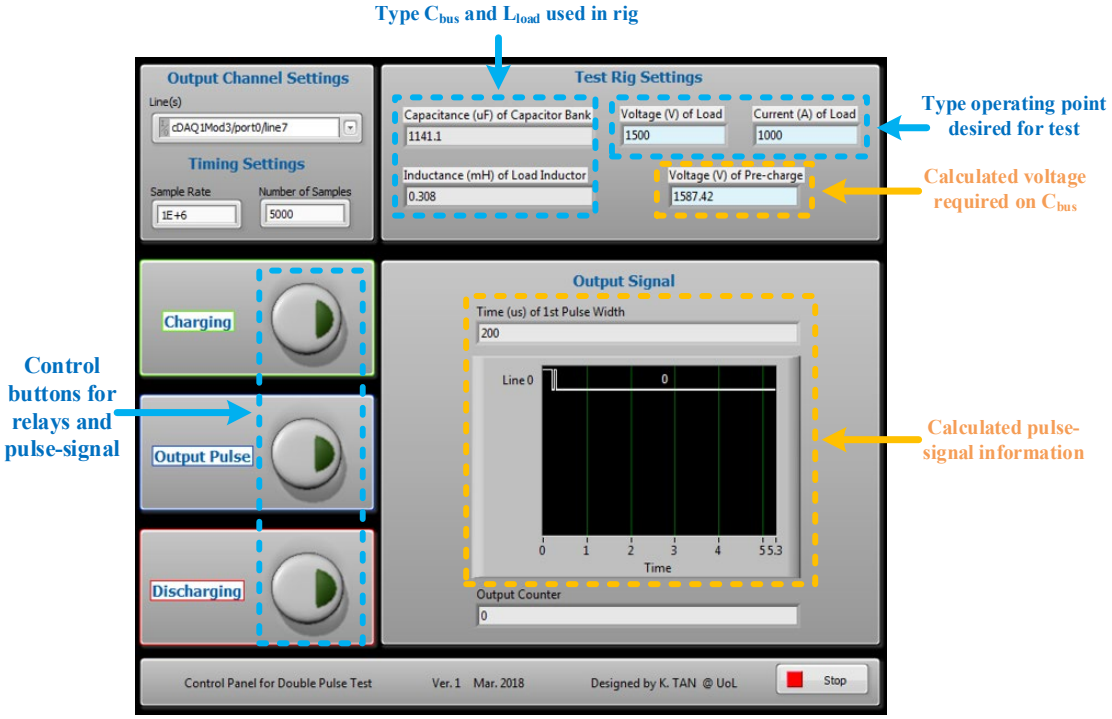


Figure 4-16: Designed LabVIEW user interface front panel for DPT platform.

The designed LabVIEW front panel for the test platform is shown in Figure 4-16. After setting the parameters of components in test rig, once the desired operating voltage and current for the DUT is typed in, the charging voltage required by capacitor bank and the output of double-pulse signal in cDAQ controller will be generated and prepared automatically. Then, simply clicking on the buttons on the left-side of panel can complete the test procedures including charging, output, and discharging. This software releases the workload of experimental operator and reduces the contacts to equipment for higher safety.

4.4.2 DPT Data Post-Processing

The switching waveforms and data captured by oscilloscope during the DPT provide the sources to extract crucial characteristics. A commonly used method to obtain this information is using cursors and math functions on the oscilloscope directly. However, this method could be laborious and time-consuming when more parameters demanded for each test. Despite of the huge workload, human error might be introduced to cause discrepancies in the results and lead to incorrect conclusion when analysing and comparing data.

With the aid of MATLAB code, the computer can extract the characteristic information in a standardised and efficient way. The current designed program can extract the parameters for both turn-on and turn-off transitions including time durations (t_d, t_r, t_f, t_{on}, t_{off}), slew rates (di/dt, dv/dt), peak values ($I_{C,pk}$, $V_{CE,pk}$), switching losses (E_{on}, E_{off}), and other values (V_m, V_{GG+}, V_{GG-}), and more functions can be further added in. All information extracted will be auto logged into Excel file for future analysis.

Filtering the random noise is crucial in obtaining accurate characteristics, especially in current and voltage peak extraction, due to the noise could be amplified for large scale measurement causing misleading results. As shown in Figure 4-18, the error introduced by random noise could get to tens of volts or amps, because the large voltage or current measured. By using a moving averaging window of 10, the noise can be filtered well to decouple the errors in parameter extraction. The detailed analysis on the random noise will be covered in the section of measurement techniques.

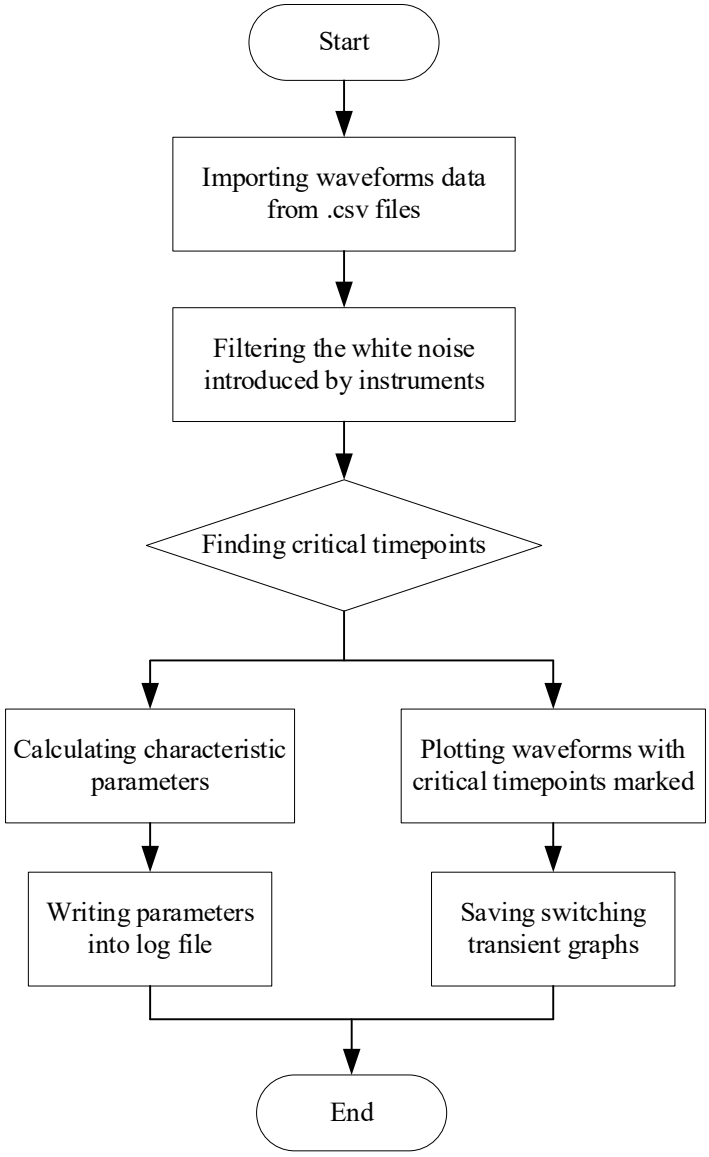
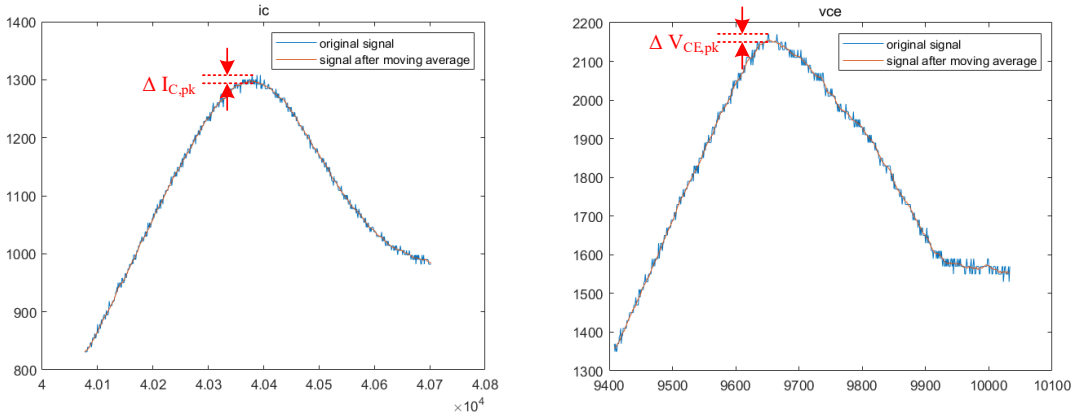


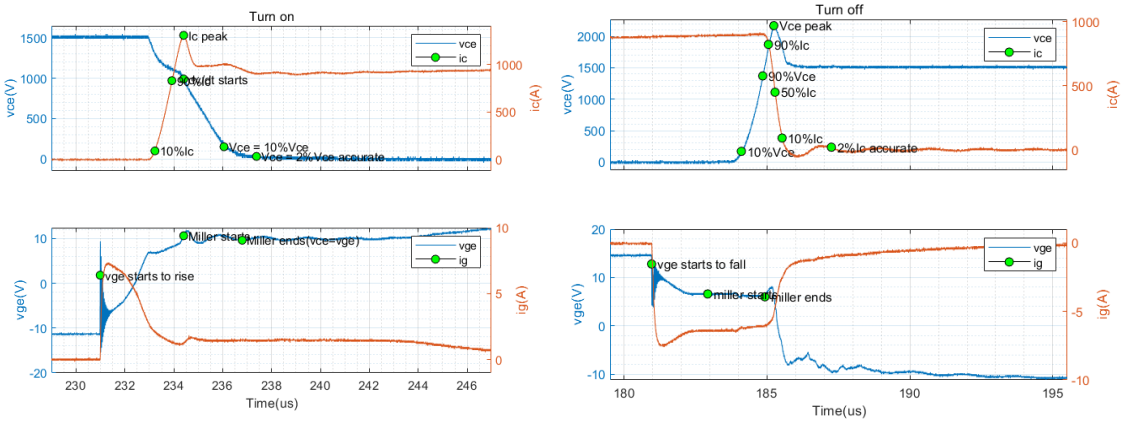
Figure 4-17: Flowchart of the data post-processing in MATLAB.



(a) *(b)*

Figure 4-18: Comparison of original and filtered waveforms of I_C and V_{CE} overshoots.

Figure 4-19 shows the auto-plotted switching transient waveforms with critical timepoints marked for parameter extraction of module FZ1500R33HE3 at 1500V/900A operating point under 2.8Ω gate driver resistor as an example.



(a) *(b)*

Figure 4-19: Auto-plotted switching waveforms with critical timepoints marked by MATLAB code.

4.5 Measurement Techniques

To accurately measure the transient switching waveforms of the IGBT module, selecting the proper instruments is necessary. In this section, the current and voltage measurement instruments will be introduced and compared firstly. Then, several aspects will be covered for accurate measurement in terms of high-frequency bandwidth, skills on setting oscilloscope, and de-skew technique.

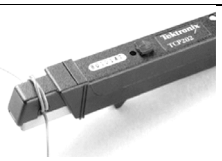
4.5.1 Current Measurement Instruments

Several instruments commonly used for current measuring on semiconductor devices including:

- Coaxial shunt
- Current transformer
- Current probe
- Rogowski coil

Table 4-3 concludes and compares these current measuring instruments.

Table 4-3 Comparison of current measuring instruments

	Coaxial shunt	Current transformer	Current probe	Rogowski coil
Appearance				
Current type	DC/AC	AC	DC/AC	AC
HF Bandwidth	Up to 2 GHz	Up to 250 MHz	Up to 120 MHz	Up to 30 MHz
Galvanic isolation	No	Yes	Yes	Yes
Price	£ hundreds	££ few thousands	£££ thousands	£ hundreds
Circuit invasion	Directly inserting impedance into circuit loop	Marginally depending on the parasitics coupled into the primary side circuit	Marginally depending on the parasitics coupled into the primary side circuit	Low insertion impedance due to the air core design
Max. measuring range limiter	Mainly depending on current flowing time, due to the limited energy dissipation on it	Saturation might occur in magnetic core for high current measurement	Saturation might occur in magnetic core for high current measurement	No saturation for air core but limited by output peak to peak voltage range

The coaxial shunt resistor applies simple mechanism of Ohm's law to convert current signal into voltage. To compare with the conventional shunt resistor, the coaxial design uses high-resistivity and thin conductor to alleviate the proximity effect and skin effect [81], and the magnetic flux produced by the current flow in the outer cylinder will be compensated by the current flow in the inner cylinder to minimise the inductance [82, 83]. However, due to its direct insertion in the power loop, the coaxial shunt has relatively large size for enough power rating, which inevitably introduces some impedance. The pulse energy dissipated on the shunt can be calculated by Equation (4-15) and must be less than the rating capacity.

$$E_{max} = R_{shunt} \int_0^T i_{(t)}{}^2 \, dt \qquad (4\text{-}15)$$

The current transformer integrated with ferrite core enables the galvanic isolation between the measuring circuit and measured current. The main limitation of utilizing current transformer is the ferromagnetic saturation caused by the DC current component.

The current probe combined both of current transformer and Hall effect sensor, which enables the capability of measuring DC and AC current simultaneously. However, it could also suffer the saturation problem to limit its current rating [81]. The current probe is better to be used for gate current I_G measurement rather than measuring collector I_C.

The Rogowski coil relies on the circular helix structure coil to pick up the induced voltage without magnetic core. Then the voltage will be integrated by the integrator to get the value of current. It has benefit in high current measurement due to the absence of saturation issue, but the large parasitics contributed by its coil structure also constrain the bandwidth [84]. In switching current measurement, the Rogowski coil is not considered preferentially for this reason.

From above, the coaxial shunt resistor is suitable for measuring low-side DUT, while the current transformer can be used for high-side FWD measurement due to its galvanic isolation. The gate current of the DUT can be monitored by the current probe.

4.5.2 Voltage Measurement Instruments

The three categories of voltage measurement instruments for voltage measuring on semiconductor devices including:

- Passive probe
- Differential probe
- Optical-isolated probe

Table 4-4 concludes and compares these voltage measuring instruments.

Due to the reason that the passive probe can only measure the voltage signal to ground, it is an ideal choice to measure the voltage across low-side DUT. The differential probe can be used to measure the voltage across any two points in circuit [85], e.g. the voltage across high-side FWD. In addition to the voltage rating, the high-frequency (HF) bandwidth and common mode rejection ratio (CMRR) are major criterions for the voltage probe selection. Optical-isolated probe can provide best noise immunity and is idealised for gate voltage measurement. However, the cost is significant.

Table 4-4 Comparison of voltage measuring instruments

	Passive probe	Differential probe	Optical-isolated Probe
Appearance			
Galvanic isolation	No	Yes	Yes
Max. voltage	Up to 20 kV	Up to 6 kV	Up to 2.5 kV
Common mode voltage	N.A.	Up to 6kV	60kV
CMRR	N.A.	Mediate	High
HF Bandwidth	Up to 4 GHz	Up to 500 MHz	Up to 1 GHz
Price	£ few hundreds	££ few thousands	£££ few tens of thousands
Circuit invasion	Insert impedance into circuit, a high-value resistor and small capacitor	Insert impedance into circuit, a high-value resistor and small capacitor	Insert impedance into circuit, a high-value resistor and small capacitor

4.5.3 Techniques for Accurate Measurement

4.5.3.1 *Bandwidth Consideration*

The IGBT module is able to achieve the switching transients rising/falling time with tens of nanoseconds, which will need to be measured by fast instruments. The bandwidth of

probes and oscilloscopes is related to the parameter of rise time. The rise time of a series-connected system of probe and vertical amplifier in scope is given by (4-16) [86]. The selected instrumental bandwidth should cover the predominate frequencies of signals to be measured.

$$t_{r,system} = \sqrt{t_{r,probe}^2 + t_{r,scope}^2} \tag{4-16}$$

Probes and scopes have input resistance and input capacitance to behave the single-pole low-pass RC response [85, 87]. For a series RC circuit, the elapsed time t since the applying of the supply voltage V_s has correspondence with the capacitor output voltage v_o, which follows Equation (4-17), where the time constant $\tau = RC$.

$$t = -\tau \ln(1 - \frac{v_o}{V_s}) \tag{4-17}$$

As the rise time is commonly defined as the time it takes for the signal to go from 10% to 90%, it can be obtained from Equation (4-17) that

$$t_{rise} = 2.2\tau \tag{4-18}$$

In addition, for the same RC circuit, the bandwidth can be calculated by Equation (4-19).

$$Bandwidth = \frac{1}{2\pi\tau} \tag{4-19}$$

Therefore, to combine Equations (4-18) and (4-19), a useful formula to converting between the bandwidth and the rise time can be obtained as

$$t_{rise} = \frac{0.35}{Bandwidth} \tag{4-20}$$

Note that the coefficient 0.35 in this formula is only available when the rise time is defined between 10 to 90 percent of signal, moreover, it is based on the system with single-pole low-pass response. In reality, the rise time specification of oscilloscopes is not quite this simple, while the 0.35 coefficient can increase to a value between 0.4 and 0.45 due to the design of steeper roll-off frequency response [85]. Therefore, when the rise time specification is not given in datasheet, the most reliable way to know the exact rise time specification is to experimentally measure it with a much faster step signal than the scope. However, for simplicity, it is still effective to use Equation (4-20) to select oscilloscope

if the "5 Times Rule" is applied. The "5 Times Rule" means that the bandwidth of selected measuring instrument should be 5 or more times larger than the highest frequency component of signal, or the rise time of selected measuring instrument should be 5 or more times smaller than the fastest rise time of signal [85]. This rule of thumb is proposed due to the approximately 30% amplitude attenuation and 45° phase shift of signal at the -3dB bandwidth frequency, which cause distorted measurement result. Thus, the "5 Times Rule" is recommended when selecting oscilloscope and probe, which achieves less than ±2% error in measurement [85]. It is always true that higher bandwidth or faster rise time of the selected measurement system will likely produce more accurate result, considering the accuracy in both of magnitude and phase [69], the "10 Times Rule" is used in this design.

4.5.3.2 *Skills on Using Oscilloscope*

The random noise aforementioned in Figure 4-18 causes errors in switching parameter extraction. There are two primary sources of noise in the measurement system as shown in Figure 4-20, which are the noise from the amplifier of active probes and the noise from the input amplifier and buffer circuits in the scope [88]. Scopes use an attenuator to vary the vertical scale factor, at the meanwhile, the noise arises after this attenuation. When the attenuator is set to be greater than 1:1 (the scope's most sensitive range), the noise will appear to be relatively larger to the signal. The same phenomenon happens when a probe with attenuation is attached to the scope.

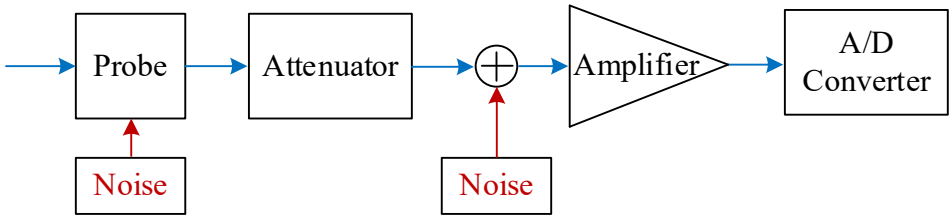


Figure 4-20: Sources of random noise in a probe-oscilloscope system.

An important tip to reduce the impact of random noise is to always expand the signal being measured to fill the whole screen on the scope. This not only minimises the amount of oscilloscope noise but also improves accuracy and resolution because of taking advantage of all of the oscilloscope's bits of resolution in analogue-to-digital converter (ADC). Experimental results in Figure 4-21 prove that the random noise is effectively

reduced by changing vertical scale on scope from 200V/div to 50V/div when taking the measurement.

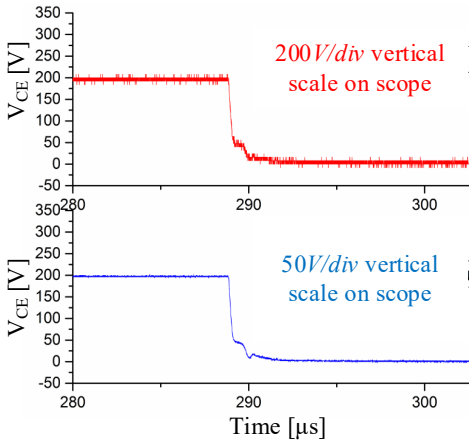


Figure 4-21: Random noise reduced by setting proper vertical scale on scope during measurement.

In addition to the vertical scale, the horizontal scaling is also important in terms of sampling rate of scope. Increasing the sampling rate as much as possible is ideal for accuracy, however, it dramatically boosts the amount of data generated during the DPT. To compromise between sampling rate and data size, the data range mainly covers duration ΔT_2 ($t_1 - t_2$) in Figure 4-3 can be saved, which contains all information of switching transient characteristics.

4.5.3.3 *De-skew of Probes*

All the measurement probes utilised in the DPT platform need to be aligned due to different signal propagation delays. The skew signals could lead to error in switching loss calculation and even incorrect transient performance in sequence in worse cases. For the semiconductor devices with higher switching speed, e.g. GaN devices, this error could be more severe [69]. For high-power IGBT modules, two switching waveforms of V_{CE} and I_C captured in the DPT is used to analyse the error caused by time misalignment. The DUT is Module FZ1500R33HE3 at 1500V/900A operating point under 1.65Ω R_G on driver. In Figure 4-22, the skew value is zero when the two signals are measured with calibration. After inserting the skew time in I_C compared with V_{CE}, the recalculated turn-on and turn-off losses deviate from the reference. The error can reach 5.2% in E_{off} when the 30ns misalignment exists, which proves the necessity of de-skew.

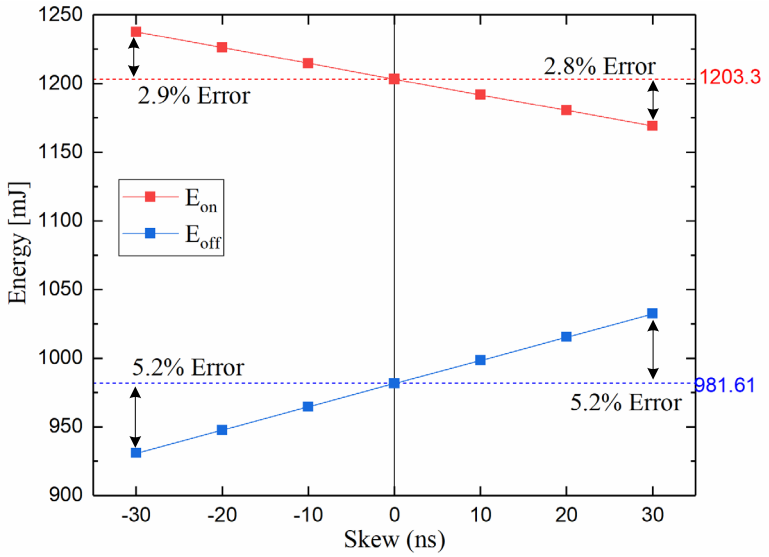


Figure 4-22: Sensitivity of switching loss calculation due to time-misalignment in current against voltage measurement.

The de-skew time of instruments equipped for the designed platform is obtained by practical calibration and concluded in Table 4-5.

Table 4-5 De-skew time for a list of instruments equipped for the designed platform

Instrument	De-skew value
Passive probe	0 ns
HV probe PPE4KV	0 ns
Differential probe P5202A	15 ns
Differential probe P5210A	10 ns
Pearson transducer	15 ns
Shunt resistor	0 ns
Current probe TCP2020	5 ns

4.6 Summary of Chapter 4

The designed double pulse test platform for high-power IGBT module is shown in Figure 4-23 and the measurement instruments are listed in Table 4-6. The proposed design method and checklist can be used to make a good compromise between the testing capability and cost. The designed computer-aided software helps to improve the efficiency and accuracy in both experiment and data post-processing. Some useful tips are also given for the sake of accurate measurement.

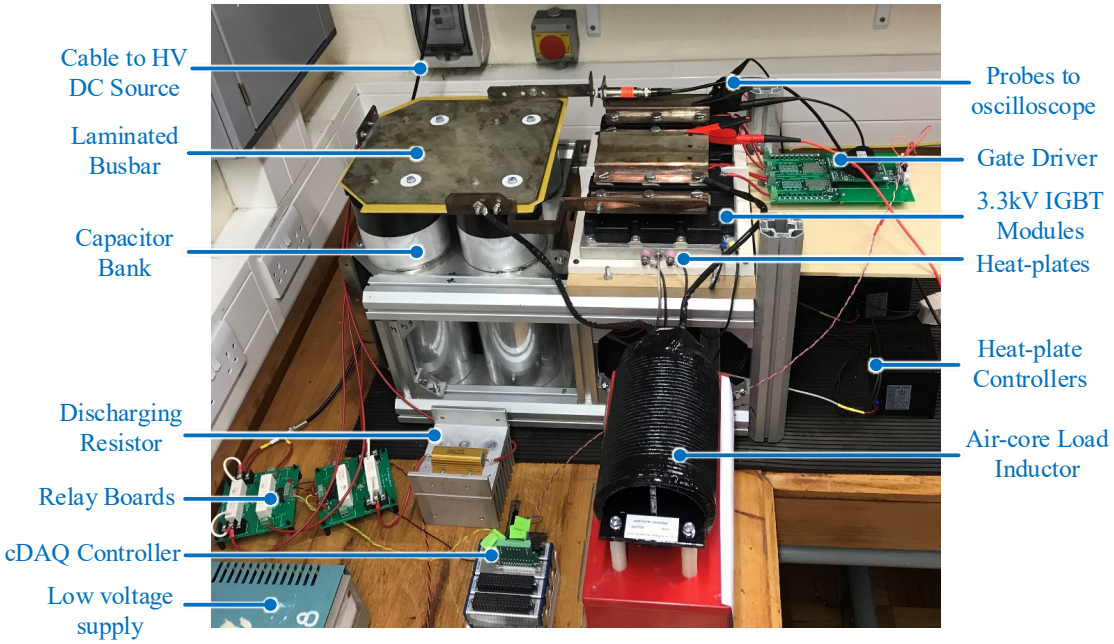


Figure 4-23: Photo of designed switching characterisation platform for 3.3kV IGBT modules.

Table 4-6 Available measuring instruments equipped for the DPT platform

Instrument	Brand	Model No.	Main Specifications
Coaxial Shunt	T&M	A-2-01	0.01 ohms; Bandpass 400 MHz; E_{max} 16 joules
Current Transformer	Pearson	6600	I*T max. 0.04 amp-sec; Bandpass 120 MHz; Output 0.1 V/A
Current Transformer	Pearson	110	I*T max. 0.5 amp-sec; Bandpass 20 MHz; Output 0.1 V/A
Differential Probe	Tektronix	P5210A	Differential Voltage 1000X: ±5600 V; Bandwidth 50 MHz
Differential Probe	Tektronix	P5202A	Differential Voltage 200X: ± 640 V; Bandwidth 100 MHz
High Voltage Probe	LeCroy	PPE4KV	Max. input voltage 4 kV; Bandwidth 400 MHz
Passive Probe	Tektronix	P2220	Max. input voltage 300V; Bandwidth 200 MHz
Oscilloscope	Tektronix	TDS7054	Bandwidth 500 MHz; 4 channels

CHAPTER 5

Proposed Gate Driver

In this chapter, an intelligent digital gate driver concept is introduced firstly. In order to realise active driving circuit, the candidate driving parameters are evaluated and compared by simulation and experiment. An active current-source gate driver topology is proposed with advantages in high flexibility of output current adjustment, fast response speed, low cost, and circuit similarity for future integration.

5.1 Overview of Proposed Gate Driver Concept

An intelligent digital gate driver can improve both efficiency and reliability at the heart of the power converters for high-power applications by combining active gate driving technology and in-situ condition monitoring. The schematic of the concept is shown in Figure 5-1, which has three main parts embedded on the gate driver board. They are the active driver circuit, on-board sensing, and on-board intelligence.

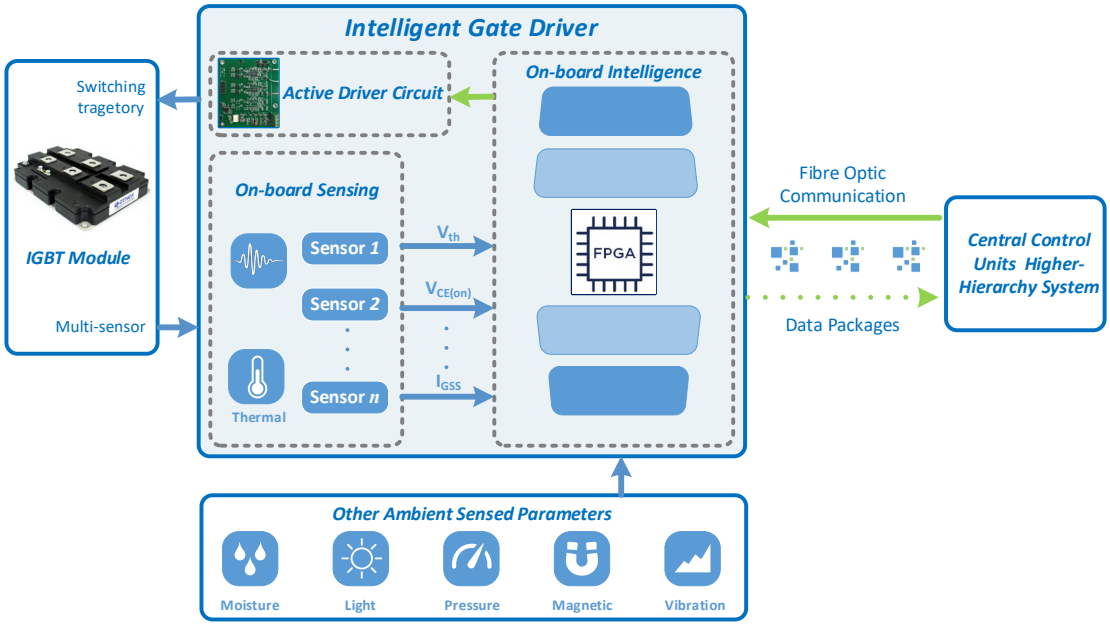


Figure 5-1: Concept of the intelligent digital gate driver for high-power IGBT modules.

The active driver circuit enables adjustment of gate driving pattern within a single turn-on/-off process or between multiple switching cycles. Each turn-on/-off process can be improved in reduced switching losses, electrical stresses and delay time compared with conventional method. Long-term failures could be postponed and mitigated by updating specific driving pattern.

The on-board sensing part measures and monitors the various parameters in addition to the event-detection and condition monitoring circuits. Parameters could be combined and extracted to uplift the sensing efficiency and efficacy and enable a timely update of adaptive gate driving profile.

The on-board processor, e.g. field-programmable gate array (FPGA), provides the local data processing capability and extracts useful features to make control decisions, in addition to communicate with a higher-hierarchy control system. The on-board digitalisation also filters the noise and guarantees that unwanted signals will not impact the whole system.

By implementing the proposed concept, the optimisation of the adjustable gate driving parameter and pattern, as well as the continuous status acquisition on device, enable a better switching performance of IGBT module in gate boosting, reduction of switching losses, and decreased transient emissions. Moreover, the given flexibility makes the gate driver to be able to self-adapt to the complex operational conditions such as electrical stress variants, environmental changes, and health degradation.

5.2 Evaluation of Driving Parameters

Based on the behaviour models and analytical expressions derived in CHAPTER 2, there are mainly three driving parameters of R_G, V_{GG} and I_G during switching stages that can be used to control the switching transient characteristics. The dependency of those important features on those driving parameters can be derived and concluded in Table 5-1, where the symbol (+) represents increase, the symbol (-) represents decrease, and (null) means non-effectiveness. Simulation has been conducted to further validate the dependency and the benefits of the active driving concepts.

Table 5-1 Overview of important features of IGBT dependency on driving parameters

	V_{GG+} (+)	$\|V_{GG-}\|$ (+)	R_G (+)	I_G (+)
t_{on}	-	+	+	-
t_{off}	+	-	+	-
E_{on}	-	null	+	-
E_{off}	null	-	+	-
$I_{C,pk}$	+	null	-	+
$V_{CE,pk}$	null	+	-	+
di/dt	+	+	-	+
dv/dt	+	+	-	+
$V_{CE(on)}$	-	null	null	null

5.2.1 Simulation of Active Gate Driving Methods

There are several electric circuit simulators currently available in market, including Spice, MATLAB Simulink, PLECS, and SIMetrix. Among them, MATLAB Simulink and PLECS are mainly used in converter-level simulation, where semiconductor devices are modelled as ideal or simplified switches with less device-level information and characteristics. To simulate the device-level characteristics, the Spice model is a common choice, which is supplied by some device manufactures. The Spice model can be imported into circuit simulators, such as PSpice and SIMetrix. However, there are still some other aspects need to be noticed when simulating switching transient of power devices.

Firstly, the level of Spice model needs to be considered. The techniques available in IGBT device modelling are introduced in [89], which can be summarised below.

- Level-0 model is a behavioural model without any real physical representation, and it is treated as an ideal switch in either on or off states. This model is simple and allows rough and fast simulation, it can be applied in the early stage of design process. It can be found in the Simulink for example.
- Level-1 model is also behavioural model, and it represents some basic properties of the IGBT devices, such as voltage drop as a function of forward current and

temperature and switching losses as a function of voltage and current. The maximum ratings are included in this model and the junction temperature is estimated by the simple multi-section RC equivalent network.

- Level-2 models are a 1-D simplified physical-properties-based system, they predict the basic physical properties and behaviour as the switching characteristics of IGBTs. The dynamic characteristics within the device can be accurately presented, except the operating area limitation.
- Level-3, -4 or -5 models are typically full physics-based. Not only can the external electrical characteristics be obtained from them, but also the internal physical and electrical information. With the higher level of modelling, the complexity increases rapidly, causing longer computational time.

Therefore, for the sake of investigating the switching transient characteristics, a relative complicated level-2 model is essential. A level-2 Spice model of the discrete IGBT device IKW40T120 from Infineon is selected.

Secondly, the convergence problem could occur when running the simulation due to the nonlinearity of IGBT model. The symptom is that the Newton-Raphson repeating series cannot converge onto a consistent set of voltages and currents [90]. One has to try to change the simulator parameters to relax the limits, which is time consuming. To relieve the influence of convergence issue, the SIMetrix software is adopted for simulation in the following sections due to its tailored simulator for power electronics with fast and reliable convergence.

5.2.1.1 *Simulation of Conventional Gate Driving*

The simulation of double pulse test is undertaken with a 500μH load inductor. The high-side IGBT is kept at off state by supplying a negative gate voltage, while the low-side IGBT is driven in a conventional manner with +15V/0V pulses and fixed gate resistor. Figure 5-2 and Figure 5-3 show the turn-on and turn-off waveforms of IGBT with various R_G ranging between 1Ω and 75Ω. The illustrated waveforms include the gate-emitter voltage V_{GE}, the collector current I_C, the collector-emitter voltage V_{CE}, the turn-on and turn-off power losses P_{on} and P_{off}, and the energy losses E_{on} and E_{off} of IGBT.

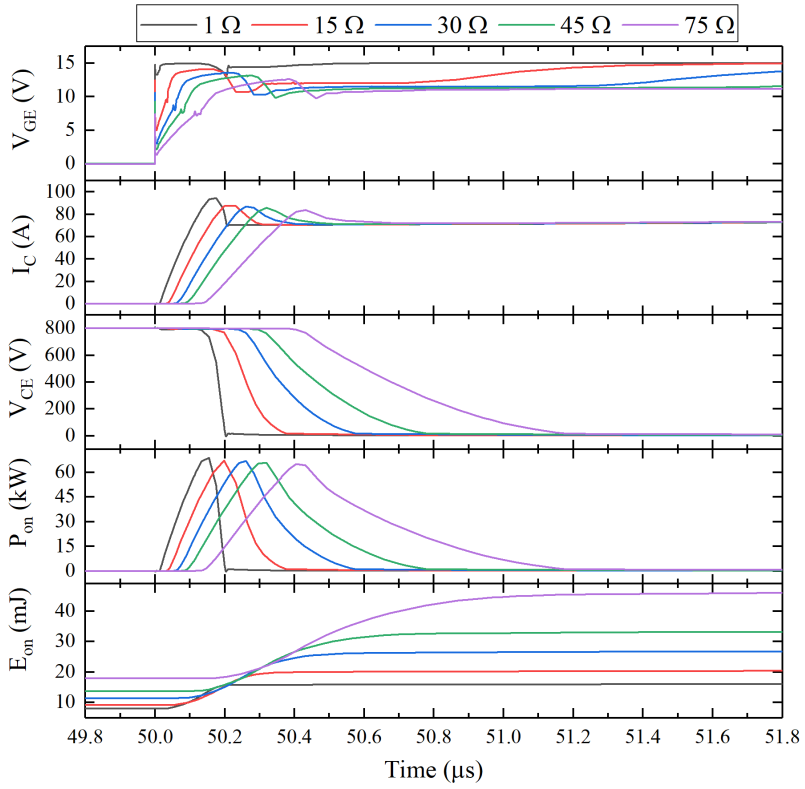


Figure 5-2: IGBT turn-on transient waveforms under various gate resistance R_G (1Ω, 15Ω, 30Ω, 45Ω, and 75Ω).

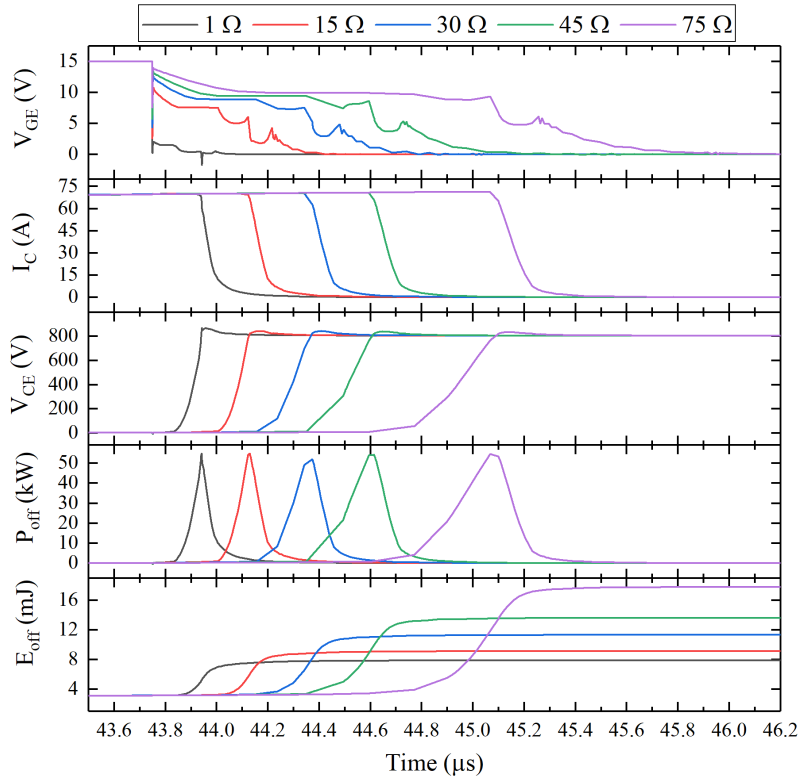


Figure 5-3: IGBT turn-off transient waveforms under various gate resistance R_G (1Ω, 15Ω, 30Ω, 45Ω, and 75Ω).

Based on the simulation results, the impact of various R_G on the key switching characteristics are concluded in Table 5-2. It can be seen clearly that with the increase of R_G, peak values of $I_{C,pk}$ and $V_{CE,pk}$ decrease, while the switching loss of E_{on} and E_{off} and the delay time of $t_{d,on}$ and $t_{d,off}$ increase. Note that the dependency aligns with Table 5-1.

Table 5-2 Key switching characteristics of CGD with various R_G

	Turn-On			Turn-Off		
R_G	$I_{C,pk}$ (A)	E_{on} (mJ)	$t_{d,on}$ (μs)	$V_{CE,pk}$ (V)	E_{off} (mJ)	$t_{d,off}$ (μs)
1Ω	94.8	7.8	0.01	865.6	4.7	0.15
15Ω	87.4	10.7	0.03	841.5	5.9	0.32
30Ω	87.1	14.8	0.06	841.2	8.1	0.55
45Ω	85.9	18.8	0.09	839.0	10.4	0.80
75Ω	83.9	27.5	0.13	833.9	14.6	1.28

5.2.1.2 *Simulation of Active Gate Resistance Driving*

This section shows the simulation results of the active gate resistance driving method. The active driving circuit of the lower IGBT now has various gate resistors can be flexibly connected into the gate loop by controlling the switches. The 1st R_G of 15Ω is used to drive the device switching on and off during most switching transient intervals, excepting a 2nd resistor R_{INT} with different resistance will be shifted in the gate loop to replace the 1st R_G during the interval of I_C commutating. Various resistance of the 2nd resistor (intermediate R_{INT}) between 1Ω and 85Ω is simulated, and turn-on and turn-off waveforms are shown in Figure 5-4 and Figure 5-5, respectively.

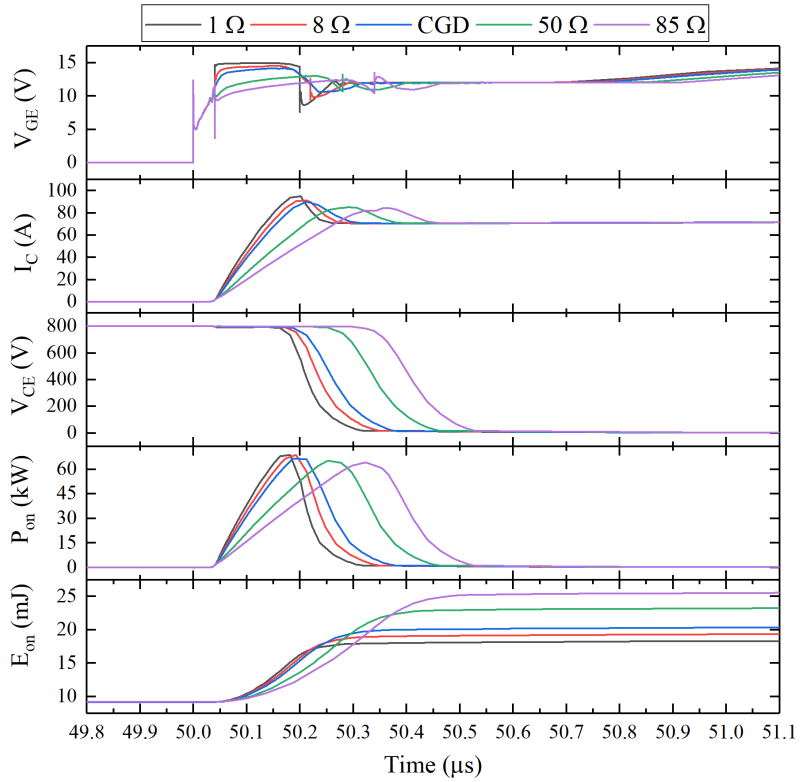


Figure 5-4: IGBT turn-on transient waveforms under various intermediate gate resistance R_{INT} (1Ω, 8Ω, 15Ω (CGD), 50Ω, and 85Ω) applied during collector current rising interval.

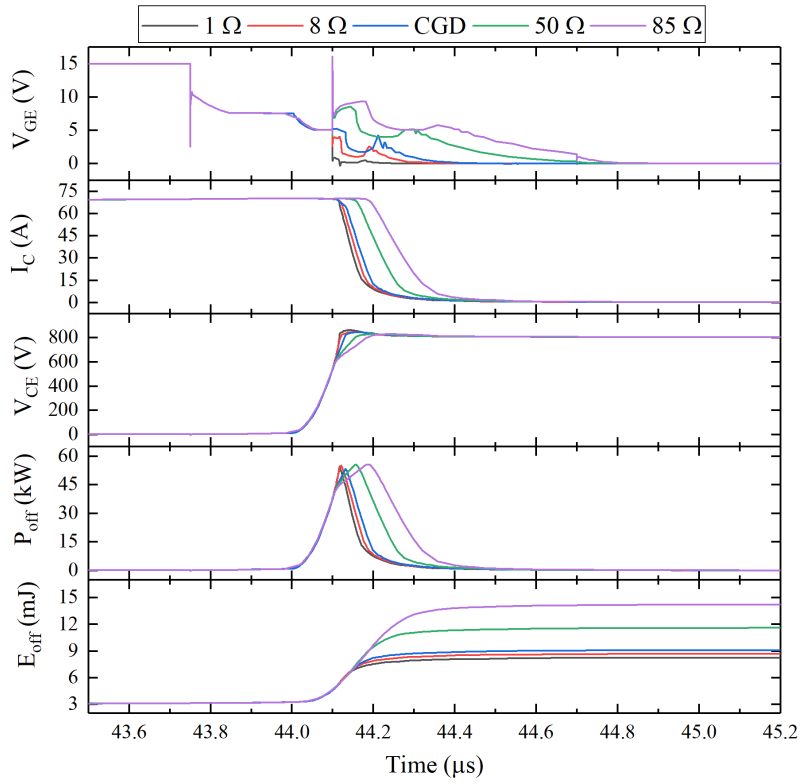


Figure 5-5: IGBT turn-off transient waveforms under various intermediate gate resistance R_{INT} (1Ω, 8Ω, 15Ω (CGD), 50Ω, and 85Ω) applied during collector current falling interval.

It can be found that the slopes of I_C are changed with different intermediate R_{INT} applied during this interval. This is due to the charging/discharging speed of V_{GE} is limited by the intermediate R_{INT} in the gate loop as shown in V_{GE} waveforms. These changes in the collector current slopes also impact $I_{C,pk}$ during turn-on and $V_{CE,pk}$ during turn-off, which are obvious in the result waveforms. On the other hand, the slopes of V_{CE} dropping in turn-on and V_{CE} rising in turn-off are almost maintained same.

Again, the important switching characteristics are concluded in the Table 5-3. It can be seen that a larger intermediate R_{INT} used, a lower $I_{C,pk}$ and $V_{CE,pk}$ are obtained, which have agreement with the trend in Table 5-1. Moreover, switching energy losses are also varied, while the delay time is maintained same.

Table 5-3 Key switching characteristics of AGD with various intermediate R_{INT}.

	Turn-On			Turn-Off		
Intermediate R_{INT}	$I_{C,pk}$ (A)	E_{on} (mJ)	$t_{d,on}$ (µs)	$V_{CE,pk}$ (V)	E_{off} (mJ)	$t_{d,off}$ (µs)
1Ω	95.1	8.8	0.03	862.4	5.0	0.4
8Ω	91.5	9.8	0.03	848.6	5.3	0.4
15Ω (CGD)	90.0	10.8	0.03	846.0	5.8	0.4
50Ω	84.7	13.7	0.03	828.5	8.2	0.4
85Ω	82.2	16.1	0.03	828.5	10.8	0.4

5.2.1.3 *Simulation of Active Gate Voltage Driving*

This section shows the simulation of the active gate voltage driving method. In the gate driver circuit, an additional voltage source is added to provide the intermediate gate voltage V_{INT}. Two switches are used to select between the original source V_{GG} and the additional source V_{INT}. The value of V_{INT} used in simulation during turn-on transition ranges between 19V and 12V, and it varies between -6V and +6V during turn-off. As shown in the waveforms in Figure 5-6 and Figure 5-7, the gate voltage waveforms of V_{GE} are influenced by various V_{INT} applied during the collector current changing during turn-on and turn-off. Hence, the switching characteristics are changed.

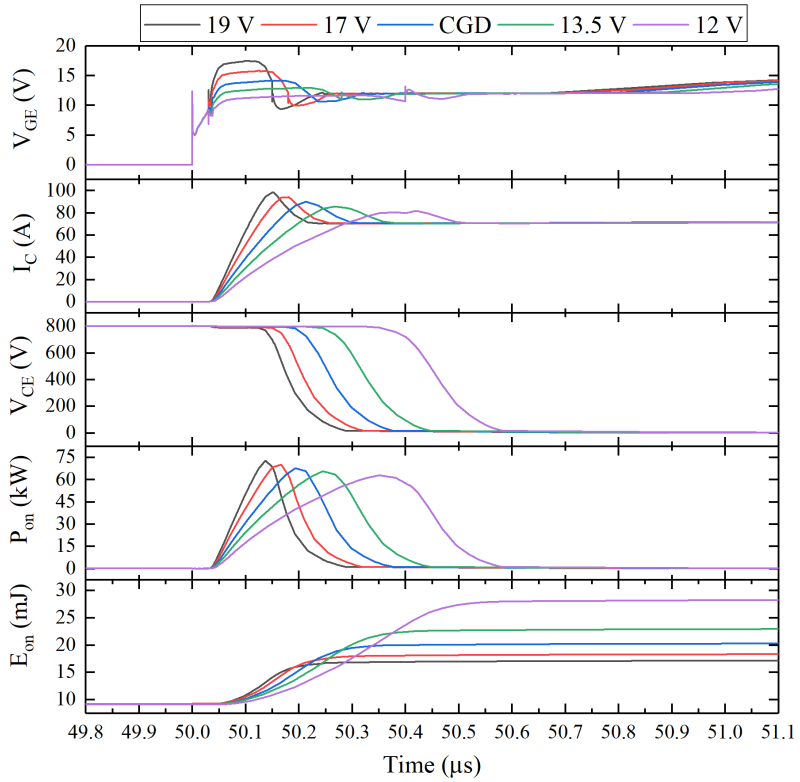


Figure 5-6: IGBT turn-on transient waveforms under various intermediate gate voltage V_{INT} (19V, 17V, 15V (CGD), 13.5V, and 12V) applied during collector current rising interval.

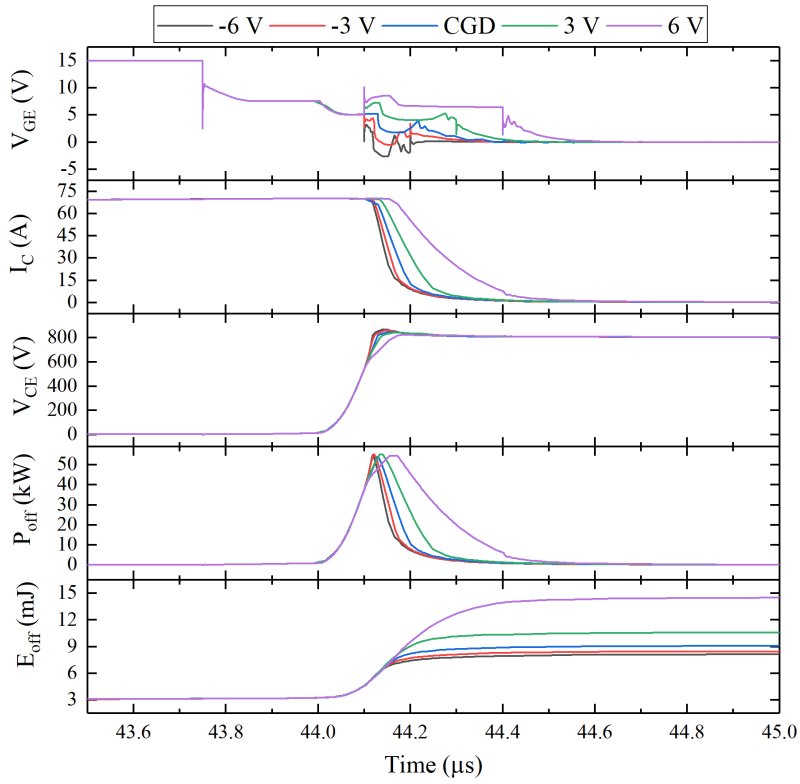


Figure 5-7: IGBT turn-off transient waveforms under various intermediate gate voltage V_{INT} (-6V, -3V, 0V (CGD), 3V, and 6V) applied during collector current falling interval.

Table 5-4 Key switching characteristics of AGD with various intermediate V_{INT}

	Turn-On				Turn-Off		
Intermediate V_{INT}	$I_{C,pk}$ (A)	E_{on} (mJ)	$t_{d,on}$ (µs)	Intermediate V_{INT}	$V_{CE,pk}$ (V)	E_{off} (mJ)	$t_{d,off}$ (µs)
12V	80.8	18.8	0.03	6V	820.1	11.2	0.4
13.5V	85.9	13.4	0.03	3V	841.4	7.2	0.4
15V (CGD)	90.0	10.8	0.03	0V (CGD)	844.9	5.7	0.4
17V	94.2	8.8	0.03	-3V	858.9	5.1	0.4
19V	98.6	7.6	0.03	-6V	867.5	4.8	0.4

According to the parameters concluded in Table 5-4, for turn-on transition, with the increment of intermediate V_{INT}, $I_{C,pk}$ is increased while E_{on} is decreased. For turn-off transition, with the increment of V_{INT}, $V_{CE,pk}$ is decreased and E_{off} is increased. The delay time of $t_{d,on}$ and $t_{d,off}$ are not influenced.

5.2.1.4 *Simulation of Active Gate Current Driving*

This section shows the simulation of the active gate current driving method. An additional voltage controlled current source is added to CGD, and switches are used to control the shifting between the conventional voltage source and the current source. Waveforms in Figure 5-8 and Figure 5-9 clearly indicate that, during the period of I_C rising or dropping, a constant intermediate current I_{INT} can influence the charging or discharging speed of V_{GE}. For turn-on transition, I_{INT} is varied between 130mA and 50mA, while I_{INT} of -80mA and -50mA are utilised for turn-off transient. According to parameters in Table 5-5, for turn-on transition, with the decrement of intermediate I_{INT}, $I_{C,pk}$ is decreased while E_{on} is increased. For turn-off transition, with the more negative value of I_{INT}, i.e. higher discharging gate current, the $V_{CE,pk}$ is increased and E_{off} is decreased. The delay time of $t_{d,on}$ and $t_{d,off}$ are not influenced.

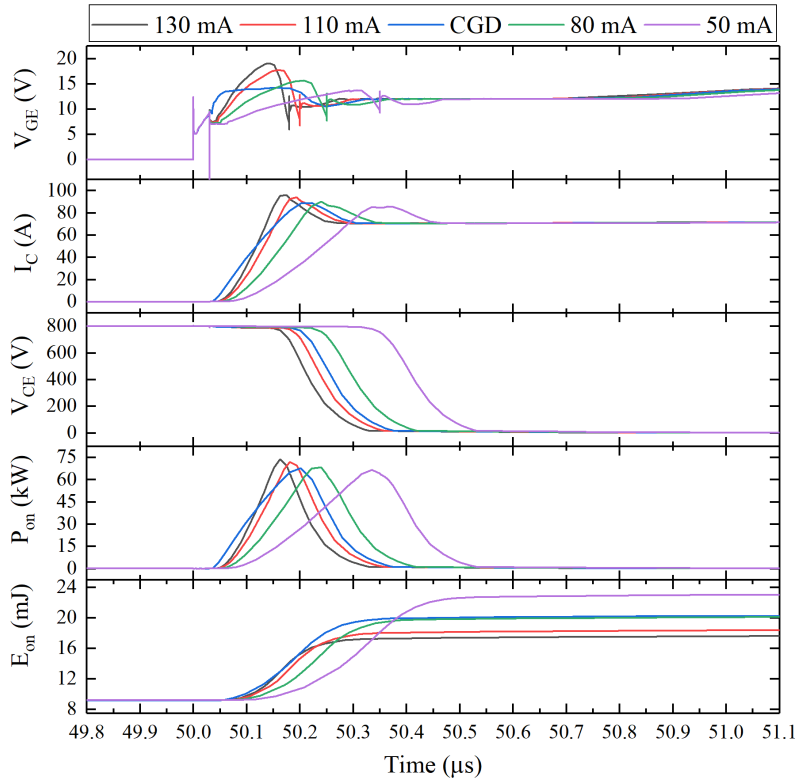


Figure 5-8: IGBT turn-on transient waveforms under various intermediate gate current I_{INT} (130mA, 110mA, 80mA, and 50mA) applied during collector current rising interval and CGD with R_G of 15Ω.

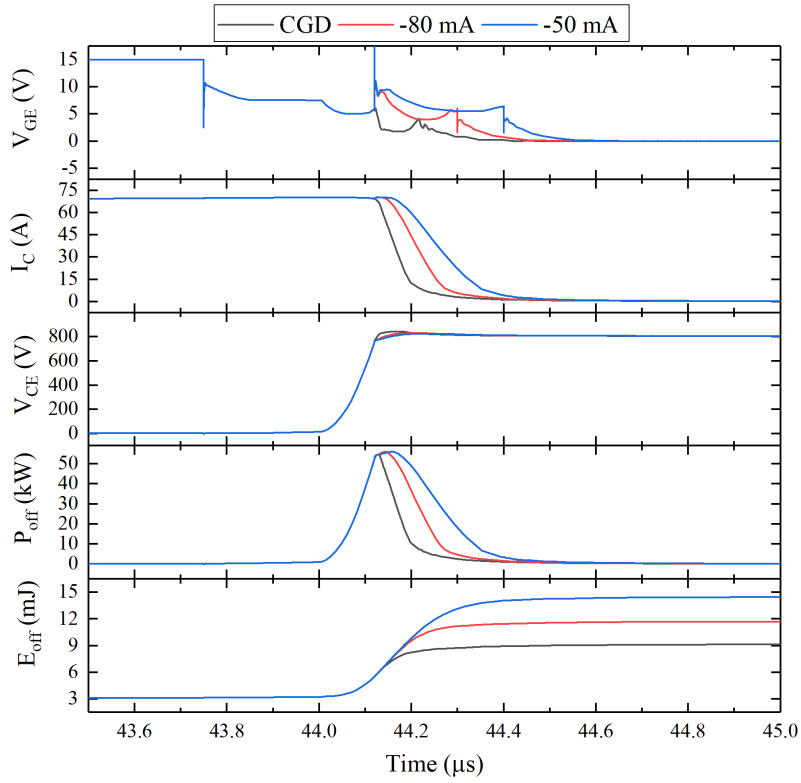


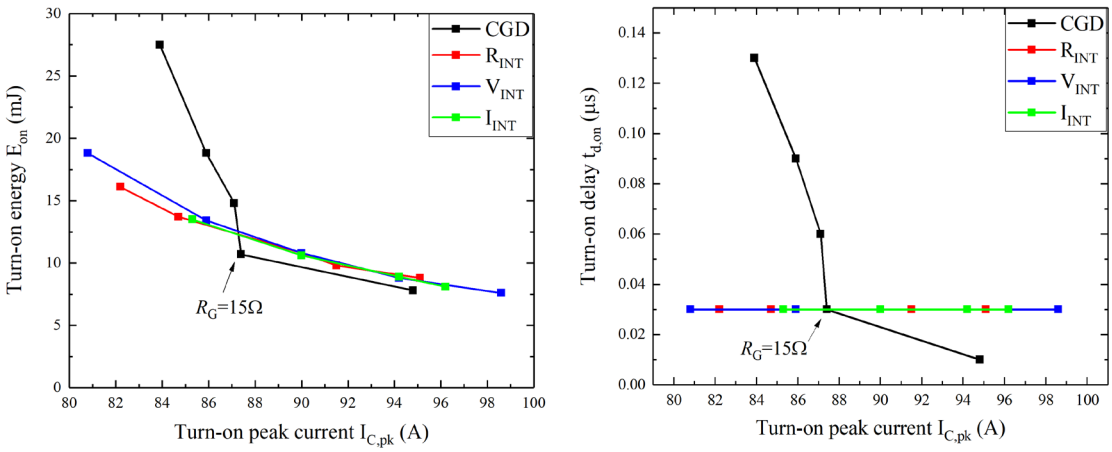
Figure 5-9: IGBT turn-off transient waveforms under various intermediate gate current I_{INT} (-80mA and -50mA) applied during collector current falling interval and CGD with R_G of 15Ω.

Table 5-5 Key switching characteristics of AGD with various intermediate I_{INT}

	Turn-On				Turn-Off		
Intermediate I_{INT}	$I_{C,pk}$ (A)	E_{on} (mJ)	$t_{d,on}$ (µs)	Intermediate I_{INT}	$V_{CE,pk}$ (V)	E_{off} (mJ)	$t_{d,off}$ (µs)
130mA	96.2	8.1	0.03	-80mA	829.9	8.5	0.39
110mA	94.2	8.9	0.03	-50mA	823.5	11.1	0.40
80mA	90.0	10.6	0.03	CGD	841.5	5.9	0.37
50mA	85.3	13.5	0.03	-	-	-	-
CGD	89.1	10.8	0.03	-	-	-	-

5.2.1.5 *Comparison of simulation results*

Comparisons between CGD and the active driving methods are shown in Figure 5-10 and Figure 5-11. For the turn-on switching characteristics in Figure 5-10 (a) and (b), the active driving methods can achieve much less E_{on} and $t_{d,on}$ at the same $I_{C,pk}$ comparing with CGD, when R_G of CGD is larger than 15Ω (on the left-hand side of marked datapoint in figures). It is worth to note that in simulations of active driving methods, only the interval of *di/dt* is actively controlled by those intermediate parameters, and the other transient intervals are still same with the CGD with 15Ω gate resistance. Therefore, when R_G of CGD is smaller than 15Ω (on the right-hand side of marked datapoint in figures), it shows less E_{on} and $t_{d,on}$. But, if other switching intervals are also controlled by the active driving methods, further improvement can be achieved comparing with CGD. Similar conclusions can be found in turn-off transition as shown in Figure 5-11.



(a) *(b)*

Figure 5-10: Comparison of CGD and different active driving methods in turn-on switching characteristics against peak current: (a) turn-on losses; (b) turn-on delay time.

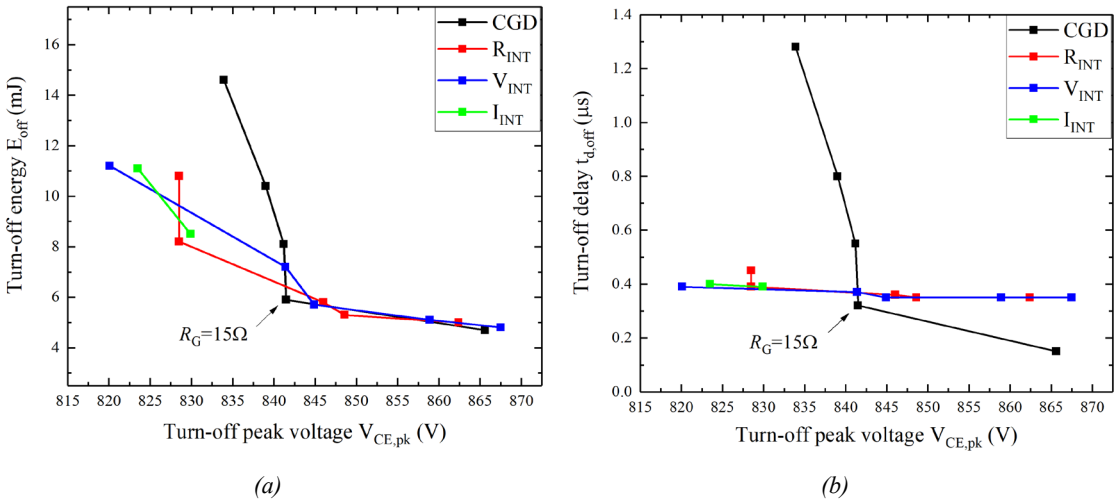


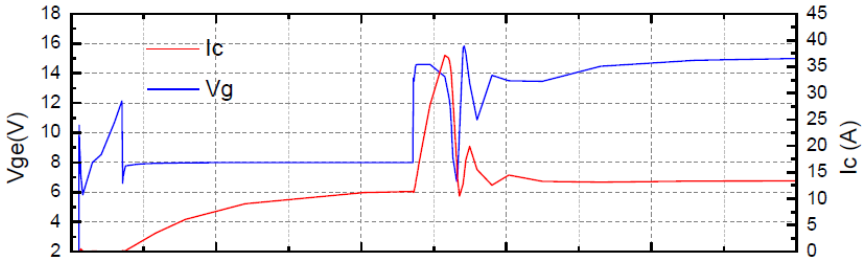
Figure 5-11: Comparison of CGD and different active driving methods in turn-off switching characteristics against peak voltage: (a) turn-off losses; (b) turn-off delay time.

5.2.2 Discussion of Driving Parameters

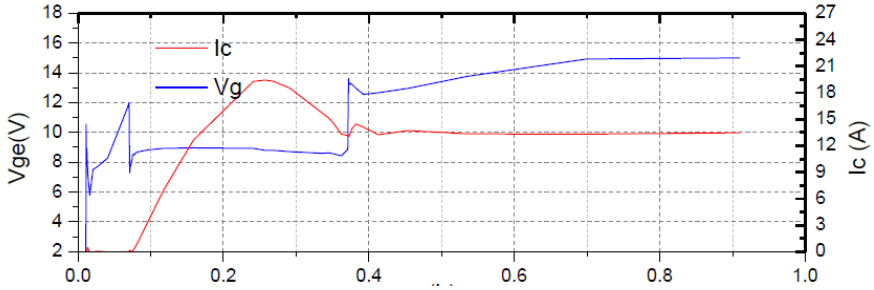
Although all three gate driving parameters of R_G, V_G, I_G are proved can be implemented in active gate driver to impact switching characteristics. There is still a lack of comparative study of them.

For the method of controlling gate voltage source V_G, which provides the required power to drive the IGBT, changing its output voltage is an obvious choice to influence the charging/discharging of input capacitor of device. However, the dynamic range of the supply voltage has restricted limitation, which is the maximum voltage of 20V that the gate oxide of IGBT can withstand. What is worse, when higher load current needs to be conducted in IGBT, a higher transient V_{GE} is required, which further narrows the supply voltage range can be selected [91]. As shown in the simulation results in Figure 5-12 (a), the intermediate voltage of 8V is applied to for the purpose of limiting *di/dt*, however, it constrains the increase of I_C because it is lower that the Miller plateau voltage required to conduct all load current. As long as it is maintained at 8V, the IGBT cannot be fully turned on, and the current spike still occur after V_{INT} is changed back to 15V. Obviously, this is not a desired control result. In Figure 5-12 (b), V_{INT} is increased to 9V to be higher than the Miller voltage under this load condition, thus the current overshoot can be effectively reduced. Therefore, the dynamic range of actively controlled gate voltage source is limited between the Miller voltage and maximum gate voltage during IGBT

turn-on. For turn-off transient, it should be limited between negative maximum gate voltage and the gate threshold voltage to avoid false turn-on.



(a) Intermediate voltage at 8V

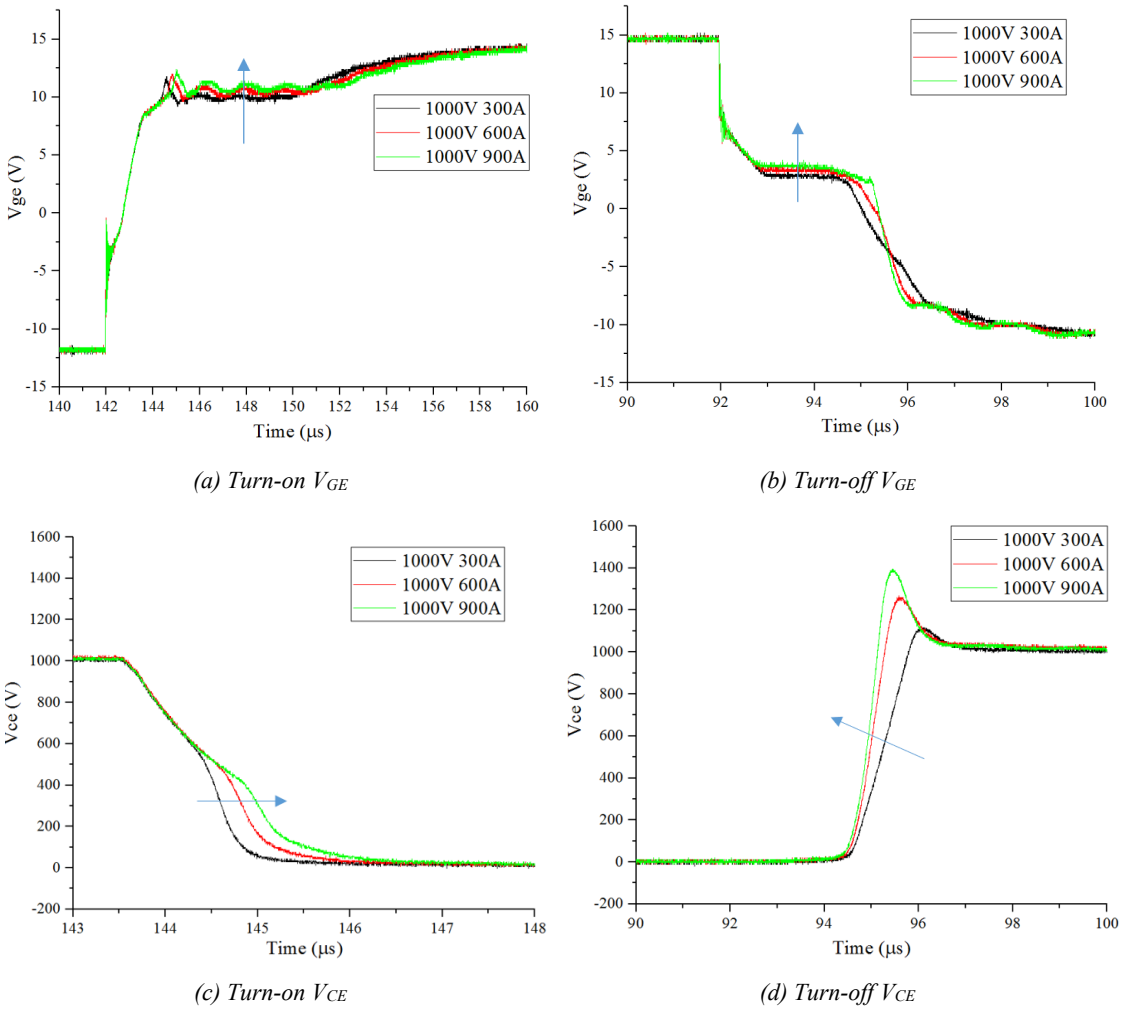


(b) Intermediate voltage at 9V

Figure 5-12: Simulation of the voltage limitation during turn-on.

Based on the above limitations, the gate voltage is not recommended for active gate driver design. Considering the gate resistance control, it is a straightforward method to be implemented based on the CGD. Adding more gate resistors controlled by switches is a relatively simple method. However, it cannot provide the unique advantageous features of current-source driving.

Firstly, the current-source driving can decouple the influences of load current on Miller voltage as mentioned in voltage-source gate driver, because it maintains constant output current under various load voltage. Experimental results of IGBT module DIM1500ESM33 driven by CGD at various load current conditions of 300A, 600A and 900A are shown in Figure 5-13. The Miller plateau voltage increases with the increasing load current as shown in Figure 5-13 (a) and (b), which leads to a lower gate charging current during the V_{CE} drop at turn-on, and a higher gate discharging current during V_{CE} rise at turn-off. Thus, *dv/dt* is influenced by the load current as shown in Figure 5-13 (c) and (d).

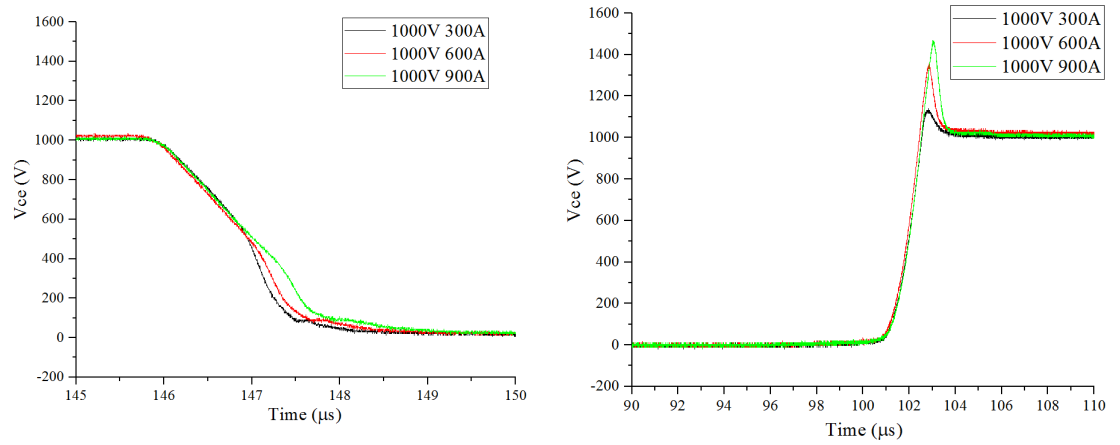


(a) Turn-on V_{GE} *(b) Turn-off V_{GE}*

(c) Turn-on V_{CE} *(d) Turn-off V_{CE}*

Figure 5-13: Miller plateau voltage increases with higher load current under CGD and its impact on V_{CE}.

To decouple the influence of load current, the current-source driver with constant output current is tested on the same IGBT module under the same conditions. The experimental results in Figure 5-14 show that the *dv/dt* is no longer influenced by the load current.



(a) Turn-on V_{CE} *(b) Turn-off V_{CE}*

Figure 5-14: The impact of load current on Miller voltage during dv/dt stage is decoupled by current-source driving.

Secondly, another advantage of controlling the gate current is that it is the most direct method to control the gate charge, which determines the switching transient characteristics. By implementing current to charge/discharge the gate of IGBT, either at fixed or dynamically changed current values, the gate charge information can be easily obtained by controller due to the charging/discharging time is already known. This feature could be used to realise advanced control algorithm.

5.3 Current-Source-Based Active Driving

Based on aforementioned benefits, the gate current I_G is selected as the most promising gate driving parameter for advanced active driving technique.

5.3.1 Design of Current Source Circuit

In order to implement the piecewise control strategy for each stage during IGBT switching transients, an adjustable output current is realised by activating a selective number of current source (CS) units arranged in an array, as shown in Figure 5-15. It consists of three main blocks, including the FPGA controller, the turn-on CSs array, and the turn-off CSs array. The FPGA has advantage in time-critical application due to its capability of parallel data processing comparing with other processors in a sequential manner. This feature is suitable for the multi-channel control signals required by the designed CSs array. The turn-on or turn-off CSs array consists of several CS circuits with same topology, which are connected in parallel. The outputs of each CS are gathered and connected to the gate terminal of IGBT. Therefore, the total output current value is determined by the number of CSs activated by the enabling signals from FPGA controller, which provides the driving flexibility for optimised driving profile.

This proposed CSs array topology has several advantages. Firstly, it provides high flexibility in setting the output current. CSs with same or different current outputs can be combined to use. Secondly, the same circuit structure of each CS makes it is to be integrated into IC for future development. Thirdly, the adjustment of output current can be implemented without using expensive high-speed digital-analogue converter (DAC).

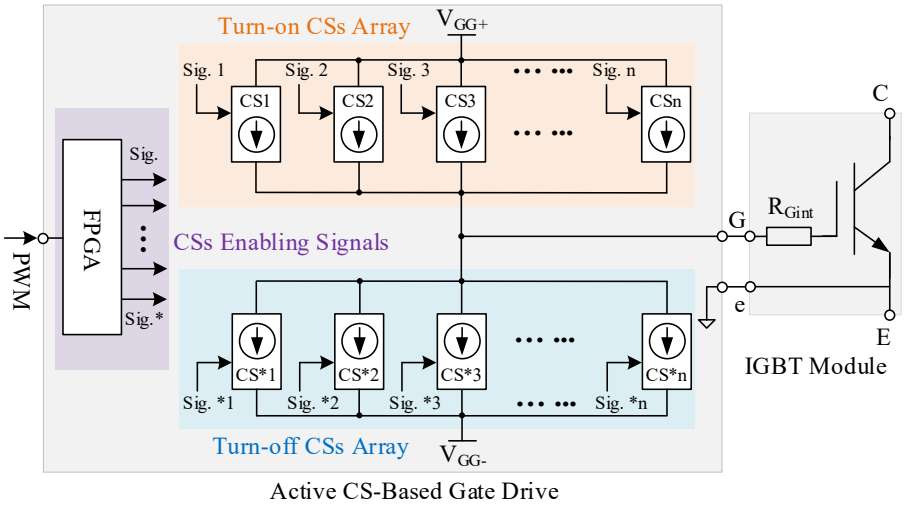
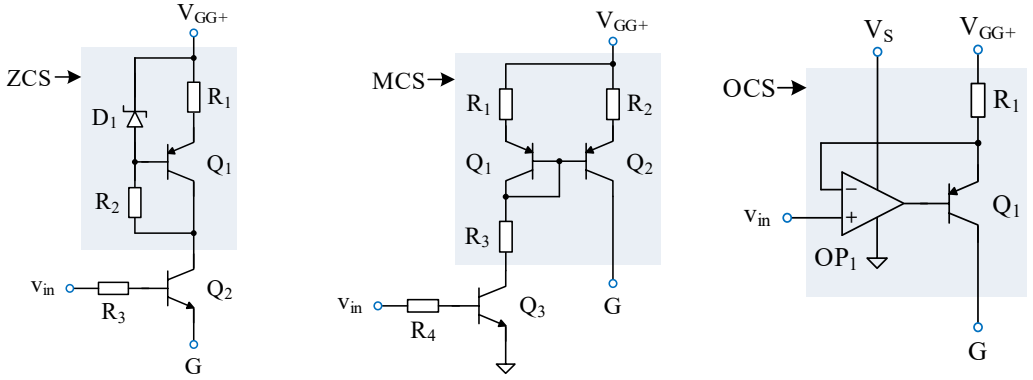


Figure 5-15: Structure of proposed active CS-based executor in gate driver.

Considering the high-power module to be driven, the CS circuit implemented in the proposed driver has some specific requirements need to be considered.

- The response speed of the CS circuit must be fast enough after receiving the enabling or disabling signal. The output current of each CS should have short delay and fast rising/falling edge to set up the desired current. The reasonable speed is required so that several on/off actions in the CS arrays can be accomplished within a single switching transition of high-power IGBT module, which normally has a switching time at μs level.
- The CS circuit must be compatible with all types of load, especially the variant capacitive load as required by the parasitic gate capacitance of IGBT. With the nonlinear variations in the parasitic capacitance and gate voltage of IGBT during switching transition, the output current of and ideal CS circuit to be adopted should be maintained a constant value and irrespective of the gate voltage changes.
- In practical circuit design, the saturation of transistors occurs to limit the working range of CS circuits to output constant current. Therefore, a reasonable compromise is that the CS circuit should avoid saturation at those important transient stages, such as (S1~S3) in turn-on and (S5~S7) in turn-off.
- A good accuracy should be achieved by the CS circuit. The tolerances in component, circuit stability, and resistance to interference should be considered. The error is inevitable in practical circuit design, but it is good if the error can be estimated.

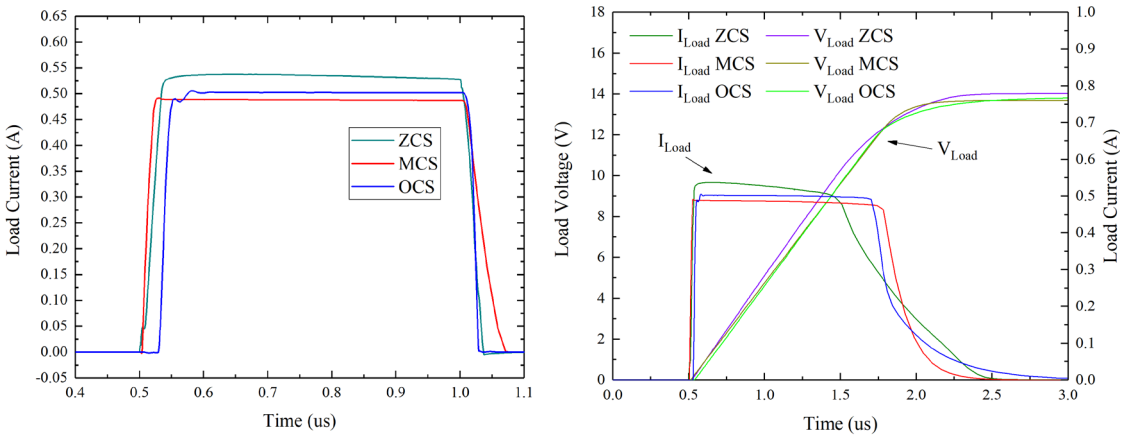
Three controlled current source topologies are investigated here to validate their capability to be applied in the active CS-based gate driver. As shown in Figure 5-16, these circuits are (a) Zener-diode-based current source (ZCS); (b) mirror-structure current source (MCS); and (c) op-amp based current source (OCS). Only the circuits applied in turn-on CSs array in Figure 5-15 have been investigated since the circuits used for turn-off CSs array have the similar structure.



(a) ZCS *(b) MCS* *(c) OCS*

Figure 5-16: Candidate of current-source topologies for CSs array in proposed gate driver.

Each CS circuit in simulation is designed to provide 0.5A output current for a 50nF capacitive load to investigate response speed and driving capability. An enabling signal with 1μs pulse width is sent to the CS circuits to examine their response speed of turn-on and turn-off. Additionally, a wider enabling signal is used to cover the full charging process of load capacitor for the sake of examining the driving capability of CSs under load voltage variation. Simulation schematics in PSpice are provided in Appendix A.



(a) *(b)*

Figure 5-17: Simulation outputs of CS circuits under capacitive load.

In Figure 5-17 (a), the results indicate that the ZCS and MCS have a quick turn-on speed at around 25ns, while the OCS is relatively slow which takes above 50ns to settle with some oscillations. For the turn-off response, the MCS takes the longest time 75ns to shut, and the other two topologies have a fast speed. Moreover, to consider the accuracy of output current, the OCS has an accurate output very close to 0.5A, while the ZCS has a relatively large error which might be contributed by the reverse current in Zener diode D1 and the base current of transistor Q2 in Figure 5-16 (a). In Figure 5-17 (b), the CS circuits' driving capability under capacitive load is shown. The results indicate that the MCS and OCS are easy to maintain a constant current output until the load voltage is charged above12V to saturation the transistors. The performance of diode in ZCS makes it a little difficult to achieve the desired load voltage before saturation, but a more sophisticated design might make it possible.

These CS circuits are also configured into the array and simulated to validate the active CS-based driving concept. The model of IGBT module CM75E3Y-24E has been used to be driven by the CS arrays. Figure 5-18 shows the gate current I_G and gate voltage V_{GE} waveforms, the gate current actively changes among 0.5A, 1A, and 1.5A before the CS saturated during turn-on transient to affect the switching characteristics.

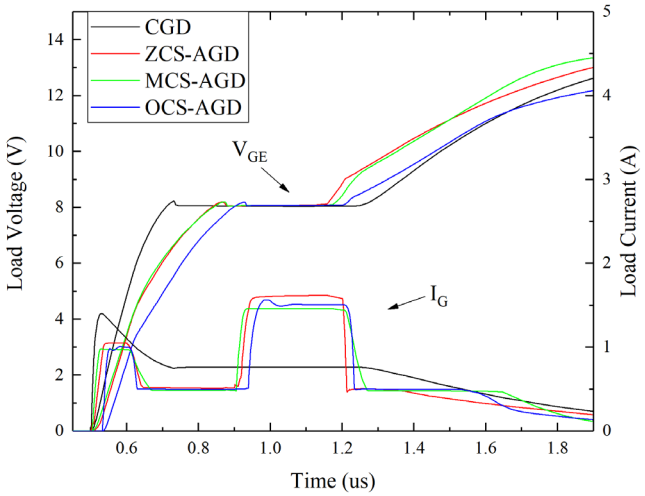


Figure 5-18: Output current and gate-emitter voltage waveforms under the control of CS arrays.

In addition to the driving capability of circuits, their ability to prevent parasitic turn-on is also examined. Figure 5-19 shows the response of different driving circuits when the crosstalk occurs, where the displacement current in Miller capacitance caused by *dv/dt* might turn the IGBT on. The effect is determined by the resistance in gate loop. The MCS

has the best anti-interference performance due to small resistance required in the gate loop, while the ZCS and OCS rely on the resistance R_1 in gate loop to set output current.

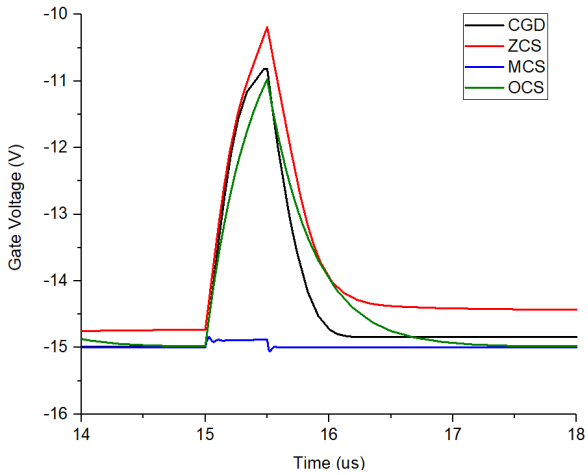


Figure 5-19: Simulation of voltage variation in different circuits during crosstalk.

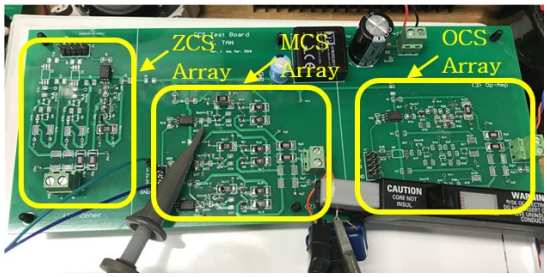
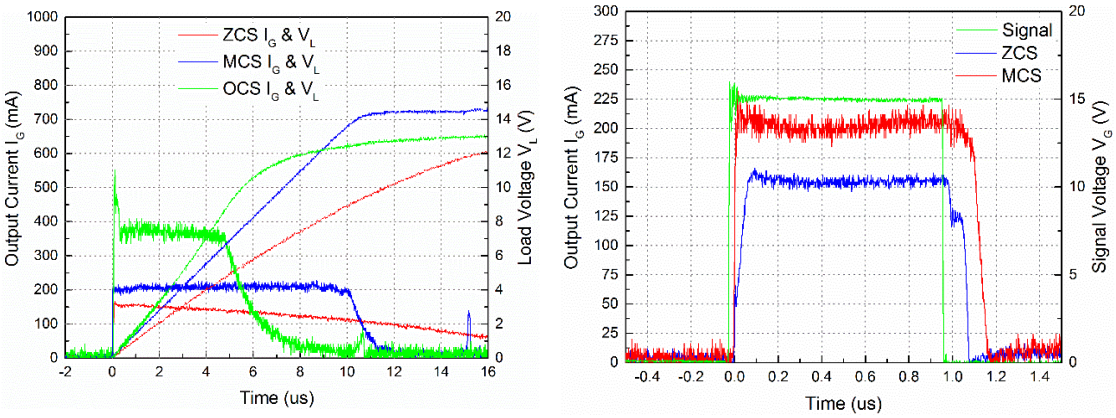


Figure 5-20: PCB for CS circuits investigation.

The three CS circuits have been designed on a PCB to experimentally investigate their performance under a 138nF capacitor load as shown in Figure 5-20. As results shown in Figure 5-21 (a), the ZCS output current has hardly maintained at constant current, where a decline in current is observed with the rise of load voltage. The decline in output current is contributed by the Zener diode, because the varying reverse voltage changes the device property. The output current of MCS is almost at the designed value to charge the capacitive load with a constant current. Additionally, a large error to compare with the designed value of 500mA is observed in the OCS, and a significant overshoot and some oscillations occur due to the parasitics and instability in the closed-loop control. Figure 5-21 (b) compares the response speed of ZCS and MCS. It is clear that the MCS has a much faster turn-on speed, while the ZCS has a better performance at turn-off. An improved design in MCS is required because it takes around 200ns to turn off, which is slow to be implemented in the proposed GD. According to the results of simulation and

experiment, the performance of the three potential CS circuits can be concluded in Table 5-6.



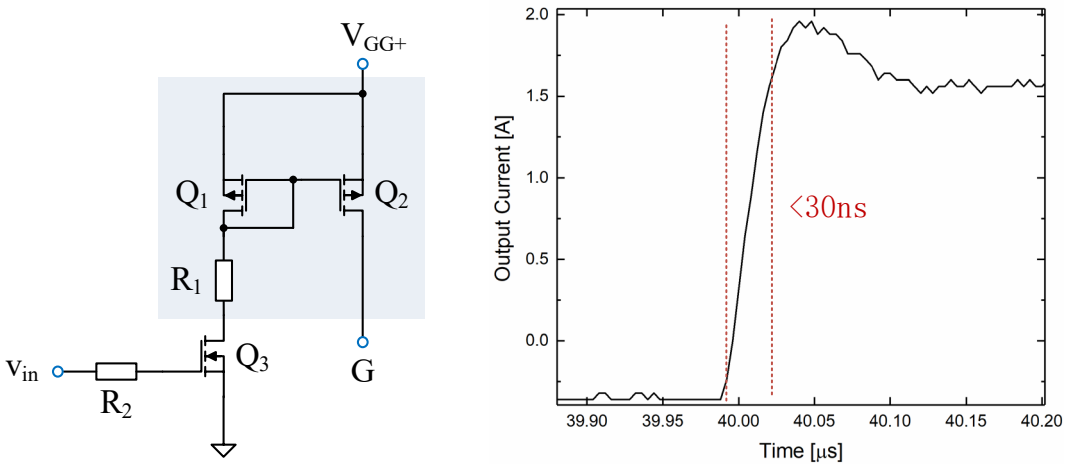
(a) *(b)*

Figure 5-21: Experimental results of output performance of the CS circuits.

Table 5-6 Comparison of CS topologies

	ZCS	MCS	OCS
ON Speed	Medium	Fast	Slow
OFF Speed	Fast	Slow	Fast
Accuracy	Low	High	High
Complexity	Simple	Simple	Complexity
Cost	Low	Low	High

The MCS topology is selected due to its overall good performance, however, its slow turn-off speed caused by bipolar transistor needs to be improved. It can be realised by implementing MOSFETs in the current-mirror circuit to replace the BJTs. The modified circuit is shown in Figure 5-22 (a). As the current-controlled device BJT is substituted by the voltage-controlled device MOSFET, the principle of the circuit is little different. Since it does not need gate current like BJT it also improves the accuracy, and the current ratio between left and right sides now depends on the device transconductance. Figure 5-22 (b) shows the experimental result at 1.5A output, the designed CS circuit still can achieve fast speed less than 30ns with high output current.



(a) *(b)*

Figure 5-22: MOSFET-based current-mirror circuit and tested output capability.

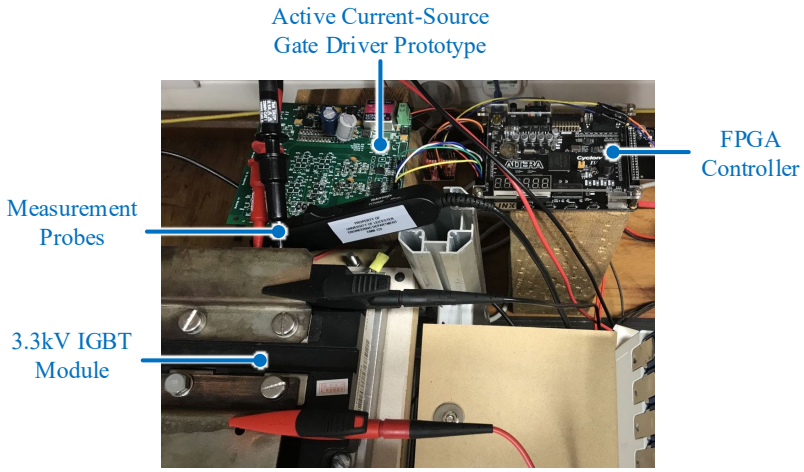


Figure 5-23: Photo of current-source gate driver prototype.

5.3.2 Experimental Results

The IGBT module FZ1500R33HE3 is driven by the proposed active current-source gate driver (ACSGD) to validate its switching transient optimisation comparing with CGD and constant current-source gate driving (CCSGD) methods. The turn-on waveforms of IGBT driven by these control methods at 500V/300A operating condition are show in Figure 5-24, including the gate current I_G, the gate-emitter voltage V_{GE}, the collector current I_C, and the collector-emitter voltage V_{CE}. It can be seen that the CCSGD supplies a constant current into the gate of IGBT without any dynamic changes, while the ACSGD's output current changes from 2A to 1A when I_C is rising. This can help to limit the current overshoot during turn-on without increasing the switching loss and time much. Switching characteristics of three methods are compared in Figure 5-25, where delay time t_d,

switching time t_{sw}, peak collector current $I_{C,pk}$, and turn-on energy loss E_{on} are all normalised for the ease of comparison. Note that these parameters are calculated according to the standard definition as introduced in Figure 2-20. Figure 5-25 proves that the ACSGD can achieve best performance than the other two methods.

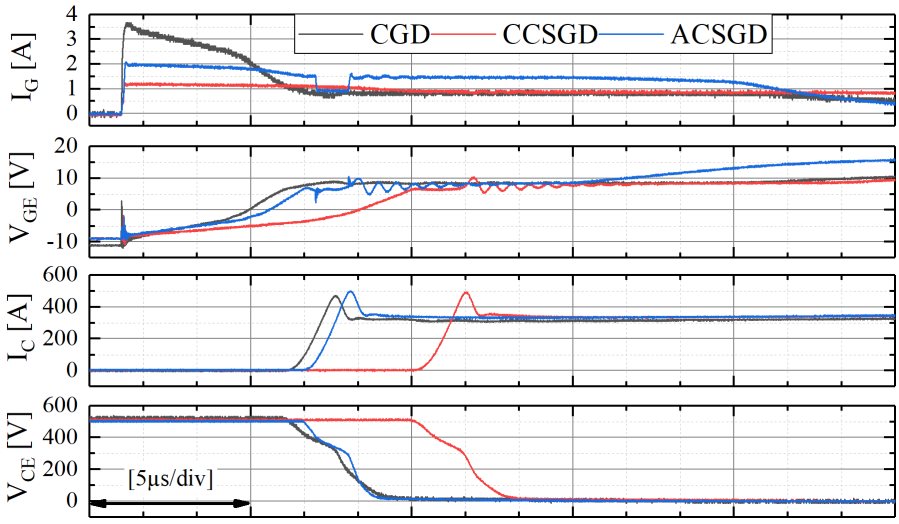


Figure 5-24: Turn-on waveforms of IGBT module driven by various driving control methods at the 500V/300A operating condition.

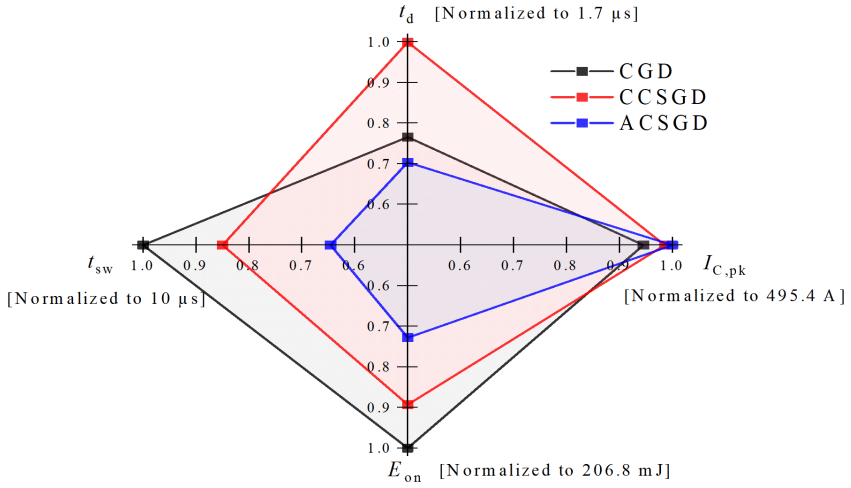


Figure 5-25: Comparison of turn-on transient characteristics of various driving control methods at the 500V/300A operating condition.

Similar comparison can be conducted at the 1000V/600A operating condition of IGBT module as shown in Figure 5-26 and Figure 5-27. The improved switching characteristics by using ACSGD can also be proved.

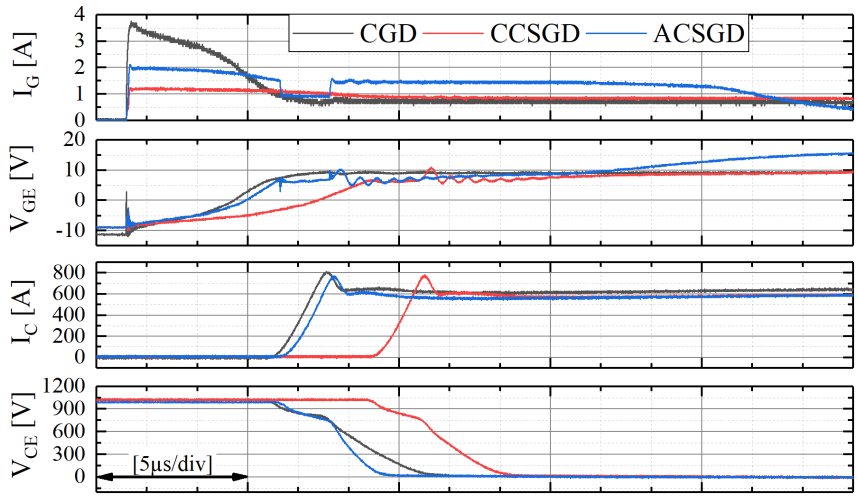


Figure 5-26: Turn-on waveforms of IGBT module driven by various driving control methods at the 1000V/600A operating condition.

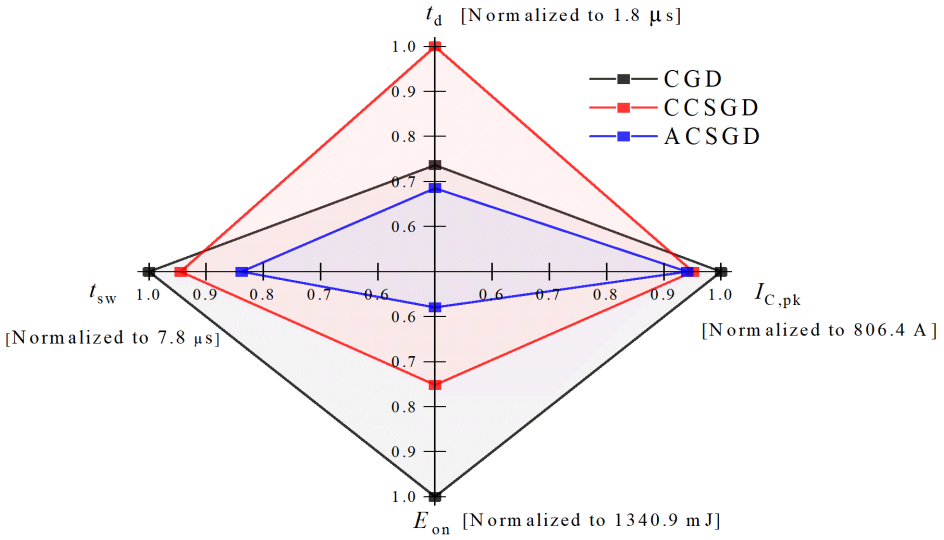


Figure 5-27: Comparison of turn-on transient characteristics of various driving control methods at the 1000V/600A operating condition.

Considering the control effectiveness of proposed ACSGD on switching transient characteristics, testing results of turn-on and turn-off transitions are concluded in Figure 5-28 and Figure 5-29 respectively. During turn-on transition, *di/dt*, *dv/dt*, $I_{C,pk}$ and *E*on are all controlled by the current value injected into gate. All the trends are aligned with the model derived in previous sections. It is similar to the turn-of transition.

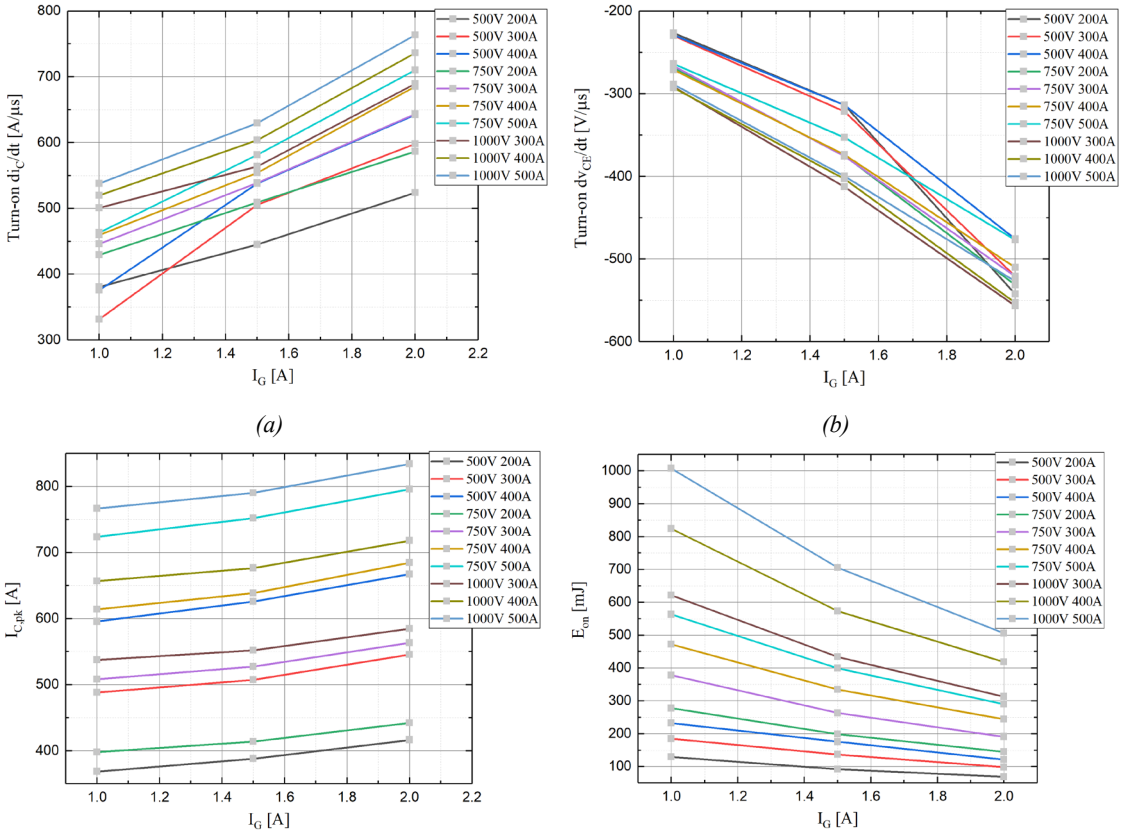


Figure 5-28: Turn-on switching characteristics controlled by output current of proposed gate driver.

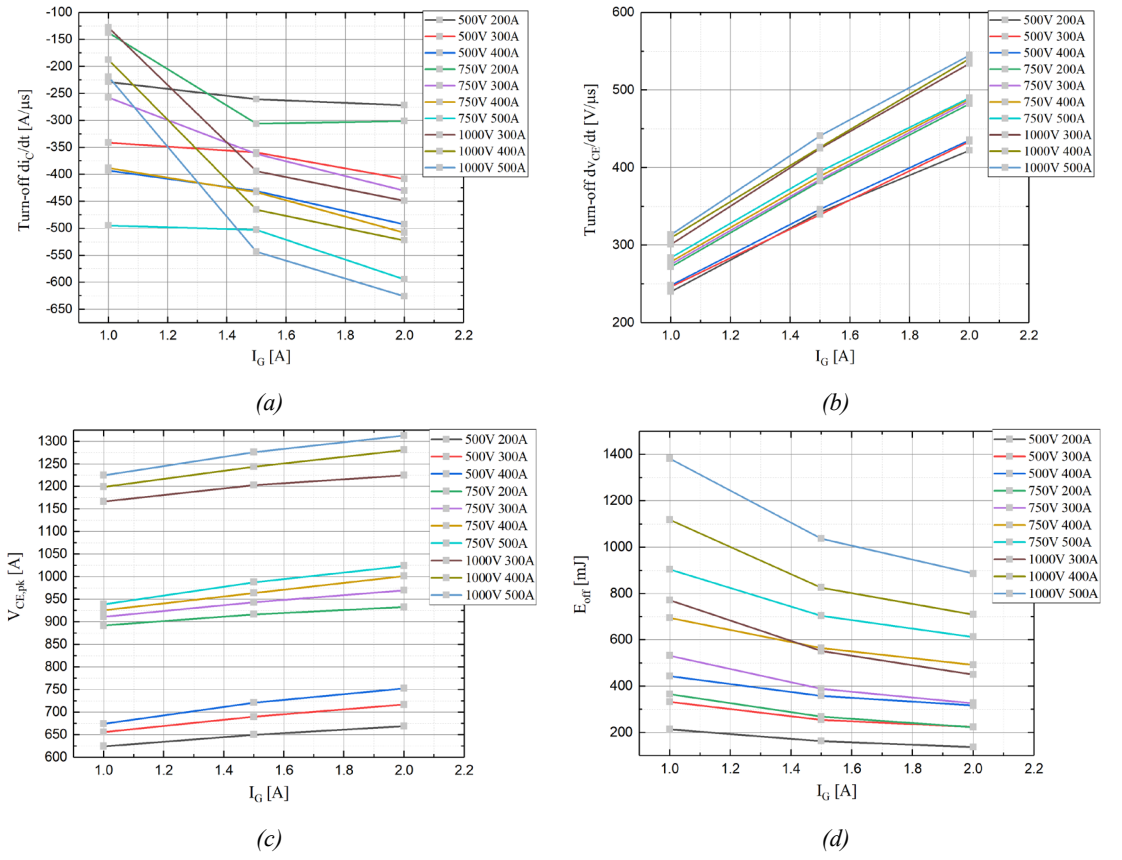


Figure 5-29: Turn-off switching characteristics controlled by output current of proposed gate driver.

To conclude, the proposed ACSGD has advantages and effectiveness in the switching transient characteristics optimisation for HV-IGBT modules.

5.4 Summary of Chapter 5

The candidate driving parameters for advanced active driving strategies are evaluated and compared. The parameter of gate current is selected as the most promising strategy. An active current-source gate driver topology is proposed with advantages in high flexibility of output current adjustment, fast response speed, low cost, and circuit similarity for future integration. The proposed gate driver is capable for the piece-wised control strategy to each switching transient stage of high-power IGBT modules. The experimental results show its effectiveness in the switching characteristics optimisation compared with the conventional driving method.

CHAPTER 6

Evaluation of Transient Controllability

The switching-edge controllability is evaluated by to what extent the collector current slope (*di/dt*) and the collector-emitter voltage slope (*dv/dt*) of the device can be regulated with the variation of gate resistance R_G. This chapter investigates the switching edge controllability of HV-IGBT modules during their turn-off transitions. Firstly, the causal relationship of transient characteristics is investigated by accounting for internal and external factors such as the on-state electric carrier distribution, the blocking voltage, the load current, and the gate resistance. Then, their impacts on the controllability are validated by simulation and experiment results. Moreover, a new method to evaluate the controllability based on the MOS-channel turn-off point on the gate-emitter voltage waveform inferring the status of internal channel is proposed. However, it is hindered by the distorted gate voltage measurement caused by internal resistance and parasitics. A calibration method is proposed for IGBT modules. At last, considerations for the improvement in its controllability is suggested for IGBT chip design.

6.1 Defective Controllability Problem

A high controllability of IGBT is beneficial to the design, which can help achieving the expected trade-off between losses and overshoot as well as EMI issues in application [92]. Otherwise, the lack of control makes it difficult to meet the rigorous industrial requirements and utilise the overall power handling capability of modules due to the derated use [14, 57]. Furthermore, the device-level controllability is also critically important for utilising advanced active gate driver techniques for optimised switching trajectory shaping and tackling the SOA reduction challenges [93].

However, advancement and modifications in the IGBT's cell structure sometimes cause defective controllability in *di/dt* and *dv/dt* during the turn-off transition [67, 94-101]. Table 6-1 summarises the previous studies on the problem, incorporating their device

information, intended control objects, tested operating points of IGBTs, and the tested range of gate resistance. The paper [97] exclusively discussed the defective *dv/dt* controllability, in which the module is tested under a range of load current, while the bus voltage is fixed. For small load current, the turn-off *dv/dt* of the module is irrespective of R_G. When the load current goes higher and R_G exceeds a certain value, *dv/dt* decreases with rising R_G. Other literature in Table 6-1 reports the lack of *di/dt* controllability during turn-off, where *di/dt* is irrespective of R_G. Even in few cases, *di/dt* increases with a higher R_G due to the carrier streaming effect [99, 100], which is in contrast to the typical relationship known between R_G and *di/dt*. However, these studies are mostly limited to low-/medium-power trench-gate IGBTs, and they were only being tested under sparse testing points. Moreover, there is a lack of study on the planar-gate designed devices, which are still widely utilised in HV application.

Table 6-1 Conclusion of literatures reporting controllability problem and testing conditions

Paper	IGBT Ratings	Chip Structure	Test Conditions	R_G Test Range	Control Object
[67]	1200V/450A	Trench-FS	600V/450A	1Ω ~ 7Ω	*di/dt*
[95]	1700V/-	Trench-FS	900V/450A	3.3Ω ~ 6.8Ω	*di/dt*
[96]	1200V/450A	Trench-FS	600V/450A	1Ω ~ 15Ω	*di/dt*
[97]	6500V/750A	Trench-FS	3600V/75; 150; 225; 300; 750; 1500A	1Ω ~ 10Ω	*dv/dt*
[98]	1200V/450A	Trench	600V/450A	1.6Ω ~ 15Ω	*di/dt*
[99]	1200V/30A	Trench-FS	100V/20A T_j=25;90;150°C	10Ω ~ 150Ω	*di/dt*
[100]	1200V/75A	-	600V/75A T_j=125°C	6Ω ~ 82Ω	*di/dt*
[101]	3300V/-(chip)	Trench-FS	1400V/60A	1Ω ~ 100Ω	di/dt

6.2 Investigation Methodology

According to aforementioned behavioural model of IGBT, the turn-off *dv/dt* and *di/dt* can be controlled by R_G, however, this impact is only existed when the MOS-channel is kept at on-state. However, an earlier MOS-channel shutdown can occur under some conditions. Between t_1 and t_2 as shown in Figure 6-1, the collector-emitter voltage V_{CE} is on the rise. During this interval, the voltage-dependent Miller capacitor C_{GC} is discharged, while the voltage v_{GE} is usually assumed as a constant V_m, which is known as the Miller plateau. However, when the gate driver supply sinks a large current from the gate terminal, C_{GE} could be forced to discharge during this interval. The C_{GC} current (i_{GC}) induced by *dv/dt* could be insufficient to meet the total gate discharging current i_G demanded. Under such conditions, the v_{GE} shows a gradual drop starting from the Miller voltage giving a discharging current i_{GE} from C_{GE} [102]. Note that the lower R_G, the higher i_G needs to be sunk from the gate.

Once the earlier MOS-channel shutdown occurs, the subsequent IGBT turn-off behaviour will be out of the gate control via R_G and thus not comply with the conventional behavioural modelling. It is entirely governed by the storage carrier extraction and recombination mechanisms that sustain the I_C inside IGBT, which can be described by the physical models studied in [102-104]. Therefore, the time point for v_{GE} crossing over the threshold voltage V_{th} is crucial, which is termed as the MOS-channel turn-off point (MTP) in Figure 6-1.

The MTP marks the transition from the gate-driver dominated area (GDA) to the intrinsic dominated area (IDA) regarding the V_{CE} and I_C switching edges control. The MTP could shift along the timeline in both directions, hence it determines to what portion of the voltage and current switching edge falls into the scope of GDA and IDA.

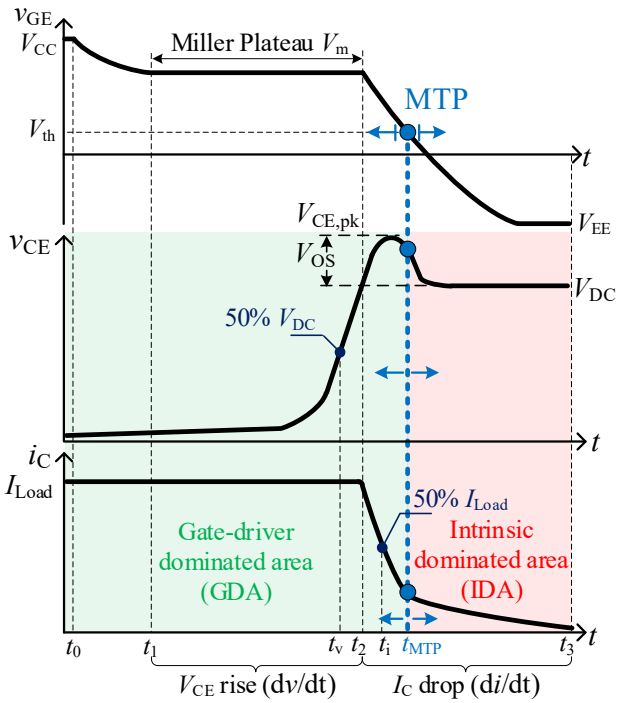


Figure 6-1: IGBT turn-off waveforms and defined areas based on the MOS-channel turn-off point.

Based on the different occurrence time of MTP, the controllability of *dv/dt* and *di/dt* can be classified into four categories, as given in Table 6-2. It is reasonable to set the midpoint (i.e. 50% of the bus voltage V_{DC} and 50% of the load current I_L) on *dv/dt* and *di/dt* slopes as the reference time points, which are named as t_v and t_i respectively, as shown in Figure 6-1.

Table 6-2 Categories of controllability status

Status	Position of MTP	*dv/dt* controllability	*di/dt* controllability
1	$t_{MTP} < t_v$	Low	Null
2	$t_v < t_{MTP} < t_2$	High	Null
3	$t_2 < t_{MTP} < t_i$	Max	Low
4	$t_{MTP} > t_i$	Max	High

Status-1 ($t_{MTP} < t_v$): It represents an early arrival of MTP during the rise of V_{CE}. In this case, the V_{CE} rising edge falls more into the scope of IDA, while the entire I_C falling edge appears in IDA as it just follows the V_{CE} rising until V_{DC}. Hence, the gate control over *dv/dt* is marginal, while the *di/dt* slope is uncontrollable.

Status-2 ($t_v < t_{MTP} < t_2$): The MTP shifts more to the right than Status-1, which enables the majority of V_{CE} rising edge falling into GDA, whereas the whole I_C falling edge

remains in IDA. Thus, the *dv/dt* parameter can be influenced by the gate driver with higher controllability than Status-1, but *di/dt* is still out of control.

Status-3 ($t_2 < t_{MTP} < t_i$): With MTP moving more rightwards compared to Status-2, the entire V_{CE} rising edge and a small portion of I_C falling edge are covered by GDA. Thus, the *dv/dt* control reaches the maximum capacity, while the *di/dt* control is marginal.

Status-4 ($t_{MTP} > t_i$): The MTP appears towards the end of I_C falling edge, thus enabling the gate driver control over both *dv/dt* and *di/dt* slopes with maximum and high controllability, respectively.

The time of MTP could be variant based on several factors, such as the on-state carrier distribution of IGBT chip, the voltage or current applied on device during the operation, which will be investigated in the following section.

6.3 Impact Factors on MTP Occurrence Time

The occurrence time of MTP can be affected by several factors, including the on-state carrier distribution of device, the bus voltage, and the load current. The physical models of IGBT have been established in the Sentaurus TCAD software to carry out the analysis of these impact factors.

6.3.1 Effects of the On-State Carrier Distribution

The CSL and the trench-gate techniques are two widely used methods to increase the on-state carrier distribution near the emitter of IGBT cells. However, this implies that more charge carrier will be stored and needs to be removed during the turn-off transition, which slows down the expansion of space charge region during V_{CE} rising [105]. Thus, the lower *dv/dt* leads to a lower current induced in C_{GC}, which can cause the earlier V_{GE} drop. This shifts the occurrence of MTP earlier and reduces the controllability of device.

Three physical models of IGBTs with different structures are developed including the trench-gate design, conventional planar-gate design, and enhanced planar-CSL. Their

simulation results of the on-state carrier density profiles are shown in Figure 6-2. It can be seen that the insertion of the CSL gives increment to the carrier concentration near the emitter, which is more than that of the conventional planar-gate design. The similar effect can be seen in the result of trench-gate IGBT as well.

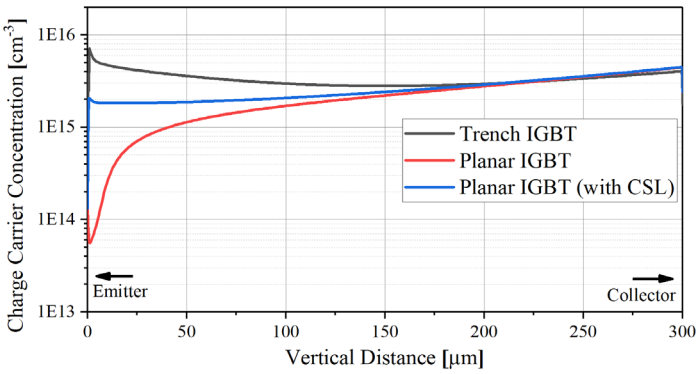


Figure 6-2: Impact of HV-IGBT structures on on-state carrier distribution.

The effect of the CSL on IGBT turn-off performance is compared between the IGBTs with and without the CSL. Figure 6-3 presents the simulation results under the operating point of 1000V/700A. It can be seen that the IGBT with CSL has a significantly slower *dv/dt* than the device without CSL. Meanwhile, its V_{GE} reaches a lower value when V_{CE} reaches the bus voltage. This can cause the early arrival of MTP when v_{GE} drops below V_{th}. A similar conclusion can be also found in the trench-gate design in [94]. Therefore, enhancing the on-state carrier density in the IGBT cell makes the IGBT prone to present lower controllability.

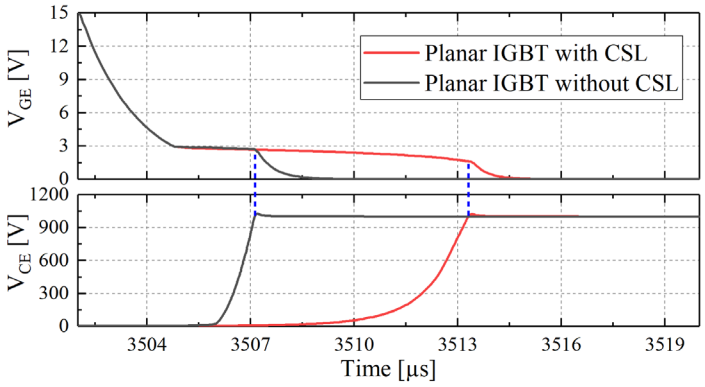


Figure 6-3: Comparison of turn-off waveforms of IGBTs with and without CSL.

6.3.2 Effects of the DC Bus Voltage

From the charge carriers' perspective, the *dv/dt* during the voltage rising can be expressed as below [105].

$$\frac{dv_{CE}}{dt} = \frac{W_N(N_D + \frac{J_{C,ON}}{qv_{sat,p}})J_{C,ON}}{\varepsilon_s P_{WNB+}} \quad (6\text{-}1)$$

where W_N is the width of N-drift region and N_D is the doing concentration, $J_{C,ON}$ is the on-state collector current density, q is the charge of an electron (1.6×10^{-19}C), $v_{sat,p}$ is the saturated drift velocity of holes, ε_s is the dielectric constant of semiconductor, and P_{WNB+} is the hole concentration of drift region at the field-stop layer interface.

As indicated by Equation (6-1), *dv/dt* is independent of V_{DC}. It is validated by the simulation results of the trench-gate IGBT model as shown in Figure 6-4. It can be seen that all the *dv/dt* slopes are aligned and irrespective of variations in V_{DC}, which are 211.1V/μs and 173.5V/μs in Figure 6-4 (a) and Figure 6-4 (b) respectively. However, a higher V_{DC} reached at the end of V_{CE} rising stage also means a smaller value of C_{GC}, which is inversely proportional to V_{CE}. Therefore, the current induced in C_{GC} is getting smaller when V_{CE} rising towards a higher V_{DC}, which will cause an earlier arrival of MTP during the turn-off of IGBT. In Figure 6-4, the higher bus voltage, the lower V_{GE} reaches when V_{CE} just rises to V_{DC}. Therefore, a higher V_{DC} causes an issue of turn-off controllability of IGBTs.

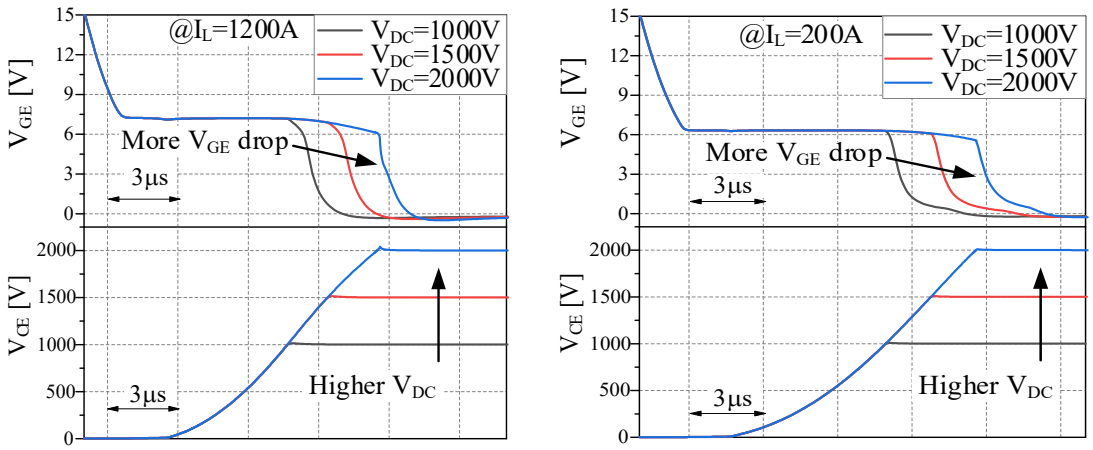
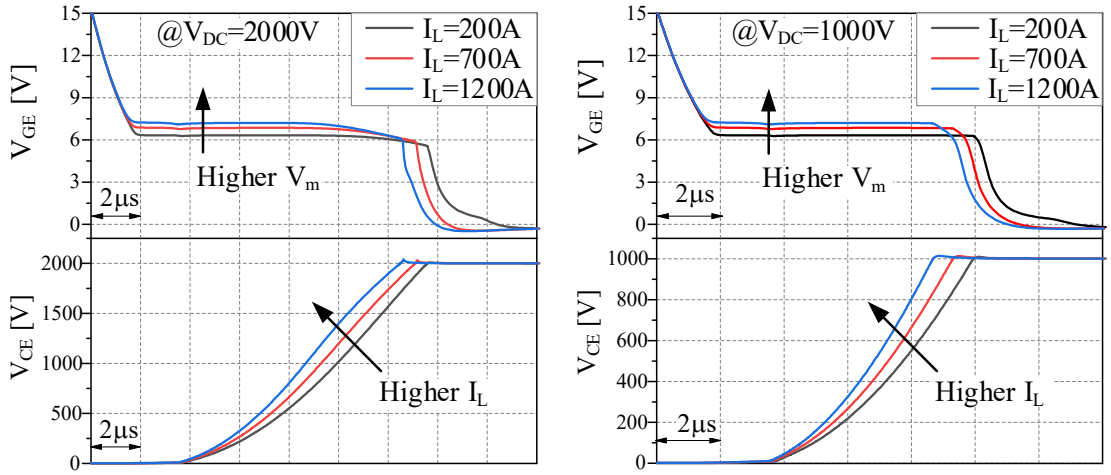


Figure 6-4: Impact of DC bus voltage on turn-off waveforms at load current of (a) 1200A; (b) 200A.

6.3.3 Effects of the Load Current

According to Equation (6-1), *dv/dt* during the turn-off transient increases with the load current (in proportional to $J_{C,ON}$). Consequently, a higher i_{GC} can be induced in C_{GC} at higher I_L conditions, which makes the sinking gate current can be easily compensated by the i_{GC} alone, without discharging C_{GE}. Additionally, as higher I_L provides a higher Miller plateau at the beginning of the V_{CE} rise stage, there is more room for V_{GE} to avoid dropping below the threshold.

Figure 6-5 presents the simulation results of the trench-gate IGBT model under various load current at 2000V and 1000V of V_{DC}, respectively. At V_{DC} of 2000V, *dv/dt* values under I_L of 200A, 700A and 1200A are 173.5V/μs, 190V/μs and 210.7V/μs, respectively. At V_{DC} of 1000V, *dv/dt* presents a similar trend. For both figures, a higher V_{GE} can be obtained under the higher I_L conditions when V_{CE} rises to V_{DC}, which validates the analysis above. Therefore, a higher I_L can postpone the arrival of MTP during turn-off process to improve the controllability of IGBTs.



(a) *(b)*

Figure 6-5: Impact of load current on turn-off waveforms at bus voltage of (a) 2000V; (b) 1000V.

6.4 Proposed Calibration in Gate-Emitter Voltage

To experimentally examine the above analysis, an accurate gate-emitter voltage measurement is the prerequisite. IGBT module incorporates different parts in its packaging, which are the sources of parasitics. Also, it comes with the internal gate resistance R_{G_int} inside package. These factors can cause the gate voltage measured at

external terminals of module is deviated from the gate voltage on internal chips. To suppress the measurement distortion, a calibration method is proposed and validated.

The equivalent circuit model incorporates an IGBT module and its external gate driver circuit is shown in Figure 6-6. The gate loop resistance involves both of R_{G_ext} on driver board and R_{G_int} inside module, while L_{com} and L_{G_loop} represent the parasitic common-emitter inductance and the parasitic gate loop inductance, respectively.

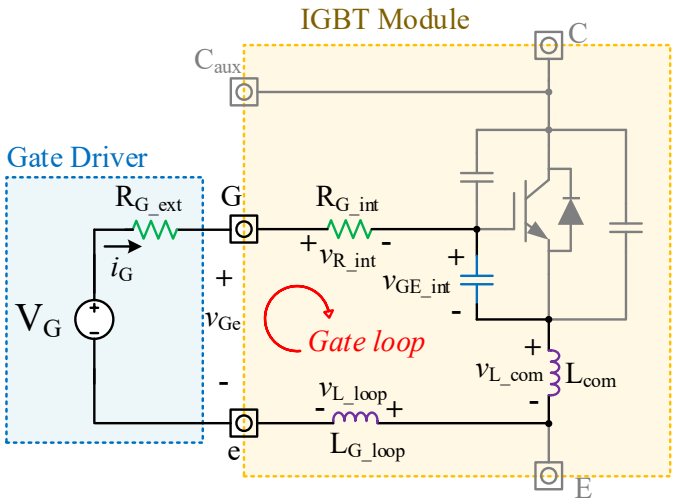


Figure 6-6: Equivalent gate-loop circuit of the IGBT module and its gate driver.

According to Kirchhoff's voltage law (KVL), the external V_{Ge} appearing across the module terminals can be expressed by Equation (6-2).

$$v_{Ge} = v_{R\_int} + v_{GE\_int} + L_{com}\left(\frac{di_C}{dt} + \frac{di_G}{dt}\right) + L_{G\_loop}\frac{di_G}{dt} \qquad (6\text{-}2)$$

These voltages are variant during switching transients, but they can be analysed in a piece-wised way. During turn-off transition, V_{CE} rises first. While I_C is kept at constant, zero voltage appears across L_{com}. Likewise, a nearly constant gate current flows during this stage, leading to zero voltage on both L_{com} and L_{G_loop}. After that, I_C and I_G starts to drop. Considering that L_{G_loop} and L_{com} values in practice and the small gate current slope, only millivolts can be induced on them. Although di/dt of I_C exists during the commutation, the auxiliary-emitter design in the module keeps L_{com} small, the induced voltage can be neglected for simplicity. Therefore, the last two terms in Equation (6-2) are ignored as shown in Equation (6-3). Similarly, it is also eligible for the turn-on transition.

$$v_{Ge} = v_{R\_int} + v_{GE\_int} \qquad (6\text{-}3)$$

Based on circuit analysis, it is easy to obtain the Equations (6-4) and (6-5) below.

$$v_{R\_int} = R_{G\_int} i_G \tag{6-4}$$

$$i_G = \frac{V_G - v_{GE\_int}}{R_{G\_ext} + R_{G\_int}} \tag{6-5}$$

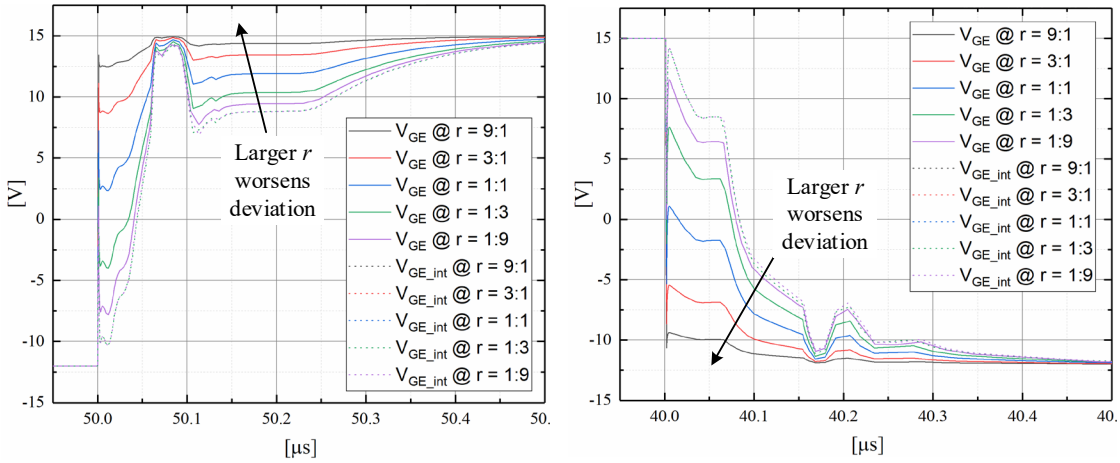
Combining Equations (6-3), (6-4) and (6-5), the absolute error between external and internal gate voltages can be expressed as

$$|\Delta v| = \left| v_{Ge} - v_{GE_{int}} \right| = \frac{r}{r+1} \left| V_G - v_{GE\_int} \right| \tag{6-6}$$

where the internal-to-external gate resistor ratio is $r = R_{G\_int}/R_{G\_ext}$.

Equation (6-6) implies that the higher the resistor ratio *r*, the worse V_{GE} distortion will be measured on module terminals. Especially for high-power IGBT modules, the ratio *r* is usually much higher than low-power devices.

Circuit simulation has been done in PSpice to validate the influence of the ratio *r*. The total gate resistance is maintained at 10 Ω, while the ratio *r* is varied between 9:1 to 1:9. Figure 6-7 demonstrates that, for both turn-on and turn-off, V_{GE} becomes more deviated from the reference V_{GE_int}, as the ratio *r* increases.



(a) *(b)*

Figure 6-7: External and internal V_{GE} waveforms under different resistance ratio at (a) turn-on; (b) turn-off.

To calibrate the externally measured gate-emitter voltage, Equation (6-7) can be used as long as the gate current waveform is also acquired.

$$v_{GE\_int} = v_{Ge} - R_{G\_int} i_G \tag{6-7}$$

The accuracy of proposed calibration method is experimentally validated on an opened 3.3kV IGBT module without silicone gel, which enables the voltage probe to be placed closing to the chip. The external V_{GE} and internal V_{GE_int} are measured under 500V/300A operating point driven by external gate resistors of 1.65Ω and 4.1Ω. The open module has an internal gate resistance R_{G_int} of 1.67Ω. A comparison is given in Figure 6-8 to firstly prove the impact of resistor ratio r. Note that the externally measured 'Miller voltage' during turn-off is negative when r equals 1, which is obviously distorted and leading to incorrect MTP finding. Moreover, the experimental results show a good agreement between calibrated and internal waveforms, which proves the effectiveness of proposed calibration method.

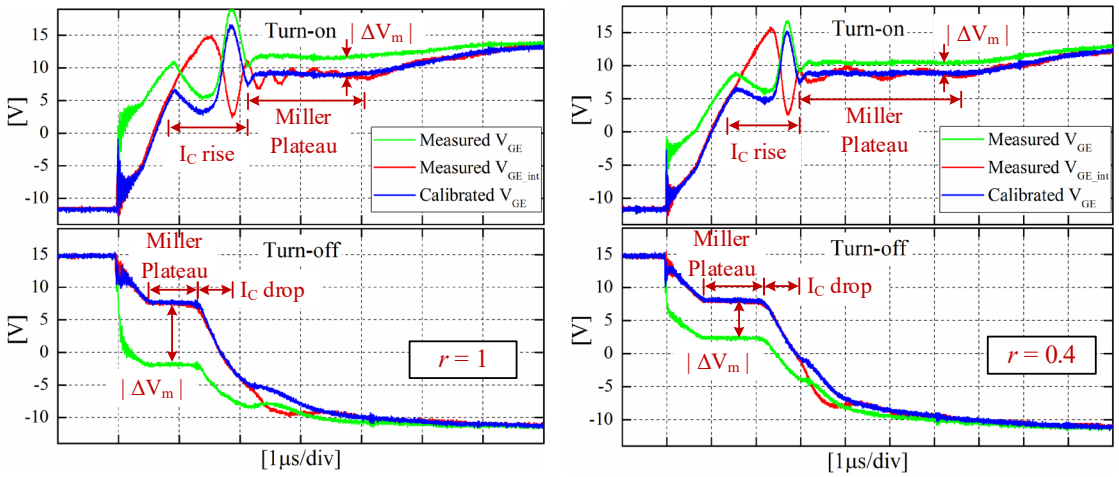


Figure 6-8: Experimentally measured and calibrated gate voltages at resistor ratio of (a) r=1; (b) r=0.4.

A minor difference can be observed on gate oscillations in Figure 6-8. The lumped inductance L_{G_loop} in Figure 6-6 is a simplified representation of the distributed parasitic inductances along the gate driving path. In practice, there are inductances in all intermediate nodes inside the module, and as shown in Figure 6-9, each raft might have different gate loop parasitics, hence causing the discordance in the measured oscillations.

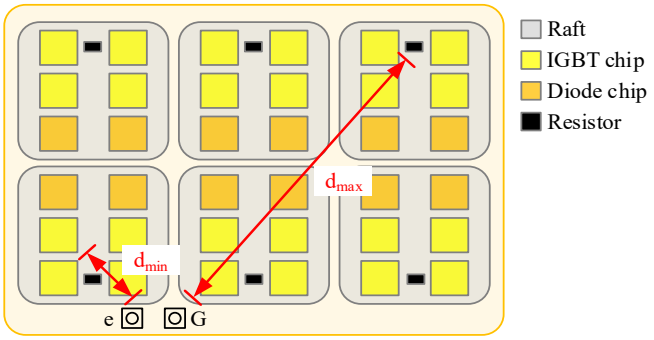


Figure 6-9: Top view of IGBT internal layout schematic

The proposed gate-emitter voltage calibration method will be used to analyse the experimentally measured turn-off behaviours of high-power IGBT modules to evaluate their controllability in the next section.

6.5 Experimental Verification

Two different types of 3.3kV/1500A IGBT modules, namely the trench-FS IGBT (Module A) and planar-CSL IGBT (Module B), are tested to investigate their turn-off controllability. Their critical parameters are listed in Table 6-3.

Table 6-3 Parameters of devices under test

Module	A	B
Chip Structure	Trench-FS	Planar-CSL
Rated Voltage	3300V	3300V
Rated Current	1500A	1500A
Internal R_{G_int}	0.42Ω	1.67Ω
Threshold V_{th}	5.8V	5.7V
Input C_{ies}	280nF	260nF
Reverse transfer C_{GC}	6nF	6nF

The testing range covers: the bus voltage V_{DC} of 500V, 1000V, and 1500V; the load current I_L of 300A, 600A, and 900A; the operating temperature T_j of 25 °C, 50 °C, and 75 °C. If not indicated specifically, the default operating temperature is 25 °C.

Measurement instruments include a differential probe Tektronix P5210 for V_{CE}, a coaxial shunt T&M A-2-01 for I_C, a differential probe Tektronix P5202A for module external V_{GE}, and a current probe Tektronix TCP2020 for I_G for V_{GE} calibration based on Equation

(6-7). The de-skew has been performed to all probes to prevent the time misalignment of measured signals.

Moreover, in the following sections, the collector voltage overshoot V_{OS} is used as an alternative index to *di/dt* for the following reasons: Firstly, V_{OS} is directly proportional to *di/dt*, which is induced on the power loop inductance according to Equation (2-35), and it is vital for the safe operation. Secondly, the existence of tail current oscillations might be a noise factor to influence the *di/dt* calculation when reading desired data point.

6.5.1 Experimental Results of Trench-FS Module-A

Figure 6-10 shows the calibrated V_{GE}, the measured V_{CE} and I_C waveforms of Module-A driven by various R_{G_ext} at the 1500V/300A condition. For R_{G_ext} equals 1.65Ω, it can be found that V_{GE} just drops to the threshold at 5.8V when V_{CE} reaches the bus voltage. Therefore, the MTP distinguishes that all portion of the V_{CE} slope is covered by GDA. Meanwhile, with the R_{G_ext} increasing between 1.65Ω and 6.8Ω, all the occurrence time of MTPs is at the I_C falling stage, this also means all the V_{CE} slopes are covered by GDA. Therefore, *dv/dt* at this condition can be effectively regulated by changing R_{G_ext}.

Then, the *di/dt* controllability under the same condition can be analysed. When R_{G_ext} increases, it can be seen from Figure 6-10 that the MTP relatively shifts to right on I_C waveforms, that makes more and more I_C slope to be covered by GDA. Until 6.8Ω, the MTP just reaches the midpoint. Hence, within the tested range, the I_C slopes are mainly covered by IDA, thus *di/dt* under this condition is rarely influenced by R_{G_ext}. From above, the controllability of Module-A at the 1500V/300A condition in Figure 6-10 belongs to the Status-3 in Table 6-2.

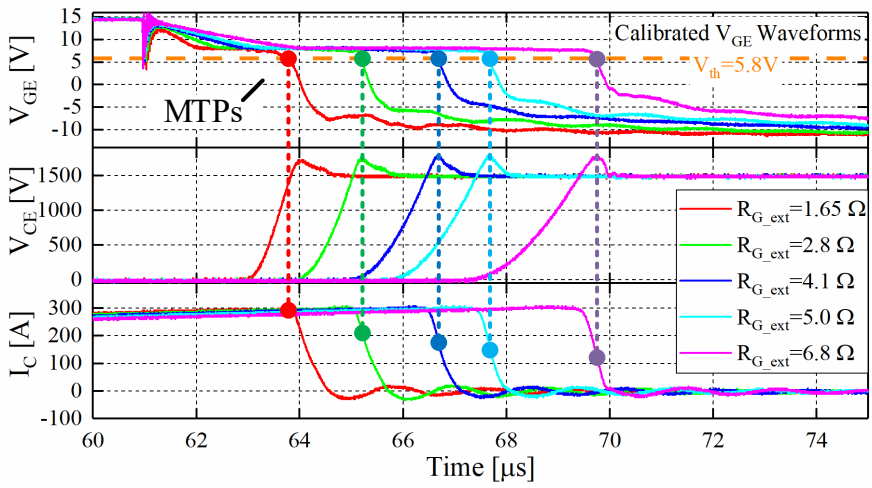


Figure 6-10: Turn-off waveforms of Module-A driven by different gate resistance at the 1500V/300A operating condition.

In Figure 6-11, the operating condition is changed to 500V/900A, while the range of R_{G_ext} is kept same. It is clear that all the occurrence time of MTPs is at the I_C falling stages, which means all the V_{CE} slopes are covered by GDA, and *dv/dt* can be effectively regulated by changing R_{G_ext}. For the I_C falling stages, comparing with Figure 6-10, all MTPs are shifted righter and major portions of I_C are covered by GDA. Therefore, *di/dt* at this condition can be effectively regulated by changing R_{G_ext}. From above, the controllability of Module-A at the 500V/900A condition in Figure 6-11 belongs to the Status-4 in Table 6-2.

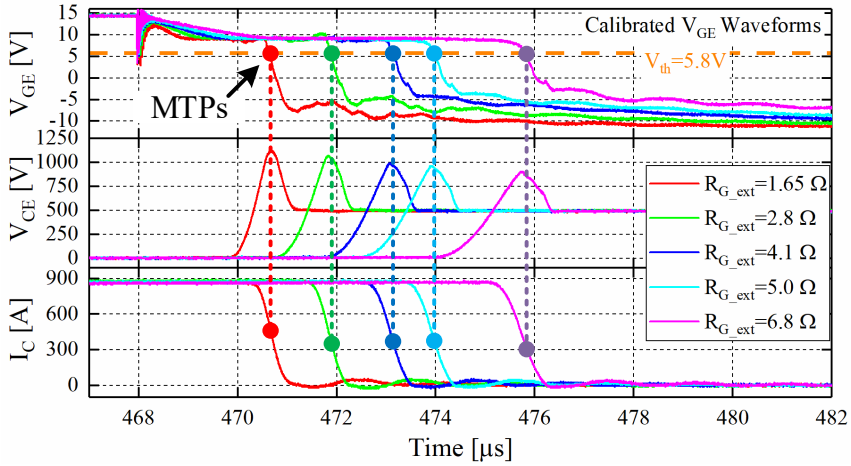
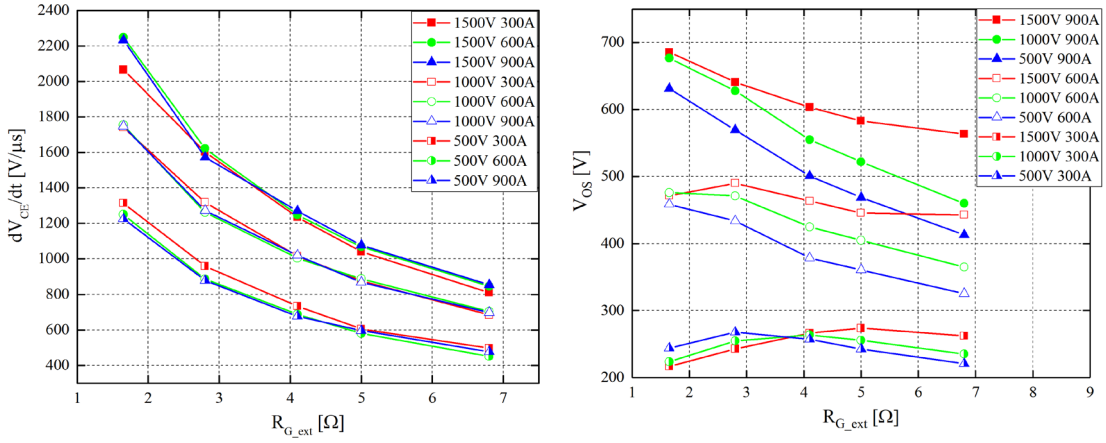


Figure 6-11: Turn-off waveforms of Module-A driven by different gate resistance at the 500V/900A operating condition.

The *dv/dt* values under all testing conditions are shown in Figure 6-12 (a), while the V_{OS} values (alternative index for *di/dt*) are shown in Figure 6-12 (b). From these figures, the controllability differences between the testing conditions of 1500V/300A in Figure 6-10

and 500V/900A in Figure 6-11 can be found. For the *dv/dt* values in Figure 6-12 (a), they can be controlled effectively by varying R_{G_ext} at both conditions. For the V_{OS} values in Figure 6-12 (b), it is obvious that the *di/dt* controllability at the condition of 500V/900A is higher than that of 1500V/300A. The results show good agreement with previous MTP analysis in Figure 6-10 and Figure 6-11 that they belong to Status-3 and Status-4, respectively. This validates the effectiveness of the MTP method.



(a) *(b)*

Figure 6-12: Turn-off characteristics of Module-A under various operating conditions: (a) dv/dt against R_{G_ext} (b) V_{OS} against R_{G_ext}.

6.5.2 Experimental Results of Planar-CSL Module-B

Figure 6-13 shows the calibrated V_{GE}, the measured V_{CE} and I_C waveforms of Module-B driven by various R_{G_ext} between 1.65Ω and 5Ω at the 1500V/300A condition. By looking at the MTPs at different R_{G_ext} values, where V_{GE} just drops to the threshold at 5.7V, all the *dv/dt* slopes only have a minor portion covered by GDA. Therefore, *dv/dt* at this condition is less controlled by changing R_{G_ext}. Considering *di/dt* under the same condition, it is irrespective of R_{G_ext} since all I_C drop stages are covered by IDA. From above, the controllability of Module-B at the 1500V/300A condition in Figure 6-13 belongs to the Status-1 in Table 6-2.

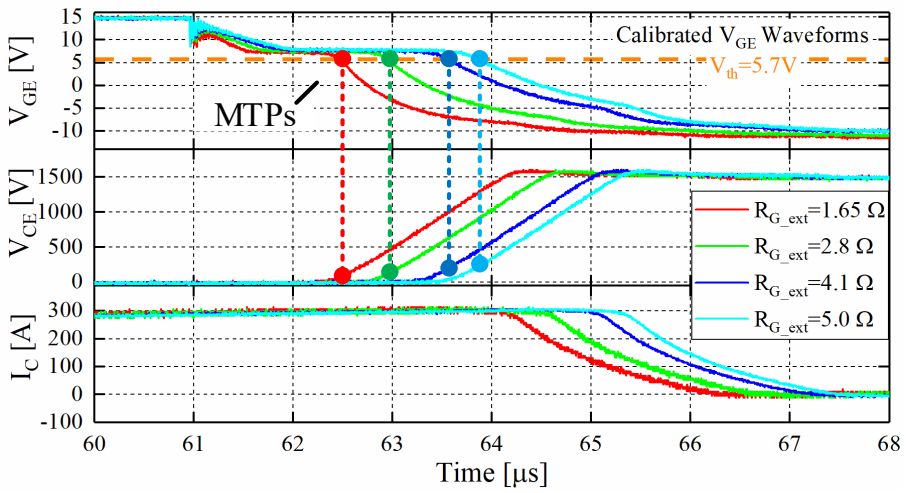


Figure 6-13: Turn-off waveforms of Module-B at the 1500V/300A operating condition.

In Figure 6-14, the operating condition is changed to 1500V/900A, while the range of R_{G_ext} is kept same. At R_{G_ext} equals 1.65Ω, the minor *dv/dt* slope is covered by GDA. But when R_{G_ext} is larger than 2.8Ω with the MTP shifts toward right, the majority of *dv/dt* slope starts to be covered by GDA. Thus, *dv/dt* at this condition is more effectively controlled by changing R_{G_ext} comparing with Figure 6-13. For *di/dt*, it is still irrespective of R_{G_ext} since all I_C drop stages are covered by IDA. From above, the controllability of Module-B at the 1500V/900A condition in Figure 6-14 belongs to the Status-2 in Table 6-2.

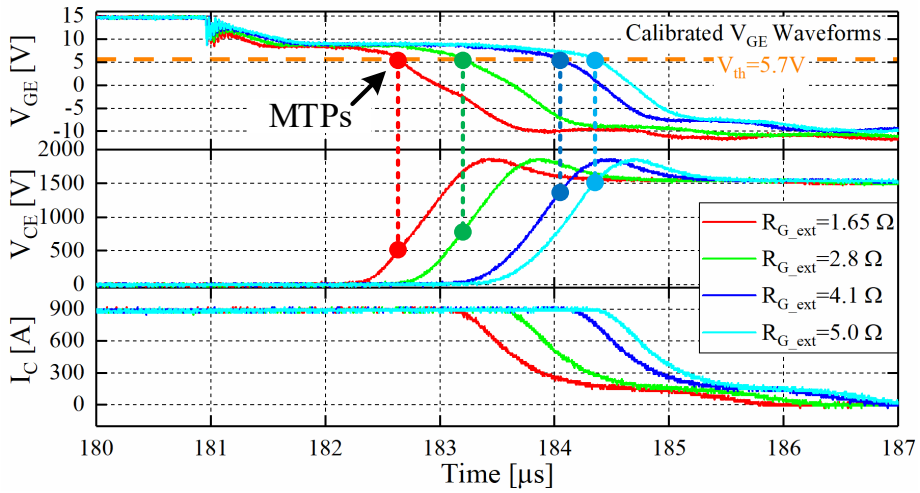


Figure 6-14: Turn-off waveforms of Module-B at the 1500V/900A operating condition.

In Figure 6-15, the operating condition is changed to 500V/900A, while the range of R_{G_ext} is kept same. It can be seen that all the MTPs are now at the I_C dropping stage, which means all the V_{CE} slopes are covered by GDA. Therefore, *dv/dt* at this condition can be

effectively regulated by changing R_{G_ext}. But for *di/dt*, the I_C slopes are still less covered by GDA, major portions are in IDA. Thus, *di/dt* under this condition is rarely influenced by R_{G_ext}. From above, the controllability of Module-B at the 500V/900A condition in Figure 6-15 belongs to the Status-3 in Table 6-2.

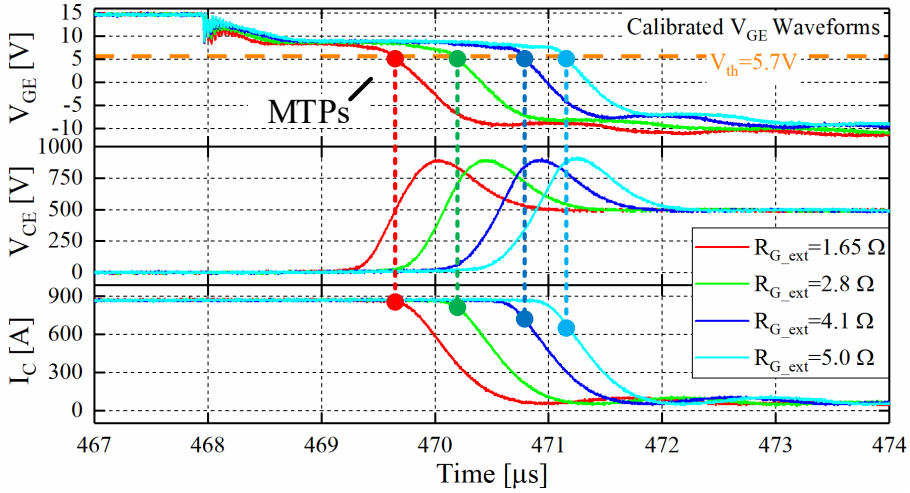
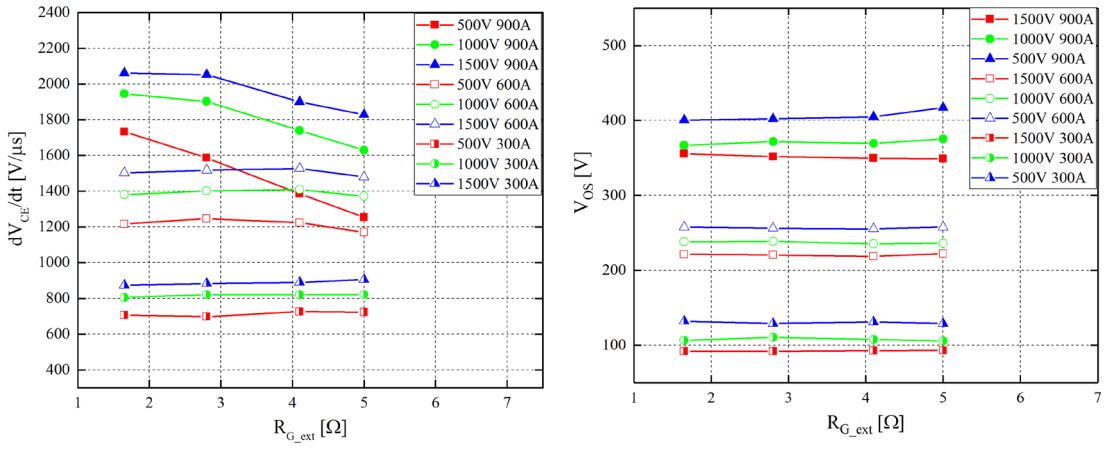


Figure 6-15: Turn-off waveforms of Module-B at the 500V/900A operating condition.

The *dv/dt* values under all testing conditions are shown in Figure 6-16 (a), while the V_{OS} values (alternative index for *di/dt*) are shown in Figure 6-16 (b). From these figures, the controllability differences among the testing conditions of 1500V/300A, 1500V/900A and 500V/900A can be found. The results show good agreement with previous MTP analysis that they belong to Status-1, Status-2, and Status-3, respectively.



(a) *(b)*

Figure 6-16: Turn-off characteristics of Module-B under various operating conditions: (a) dv/dt against R_{G_ext} (b) V_{OS} against R_{G_ext}.

6.6 Discussions on Operating Conditions and Devices

To further evaluate the impact of operating conditions of V_{DC} and I_L on the controllability of IGBTs according to the results in the previous section, the *dv/dt* controllability (i.e. $k_{dv/dt}$) and the *di/dt* controllability (i.e. k_{Vos}) are defined in Equation (6-8) and Equation (6-9) respectively,

$$k_{dv/dt} = \overline{\left(\frac{\Delta dv/dt}{\Delta R_{G\_ext}}\right)} = \frac{1}{n-1}\sum_{i=1}^{n-1}\frac{dv/dt_{(i)} - dv/dt_{(i+1)}}{R_{G\_ext(i+1)} - R_{G\_ext(i)}} \quad (6\text{-}8)$$

$$k_{Vos} = \overline{\left(\frac{\Delta V_{OS}}{\Delta R_{G\_ext}}\right)} = \frac{1}{n-1}\sum_{i=1}^{n-1}\frac{V_{OS(i)} - V_{OS(i+1)}}{R_{G\_ext(i+1)} - R_{G\_ext(i)}} \quad (6\text{-}9)$$

where n is the total number of tested gate resistors, and i is the index (e.g. $R_{G\_ext(i=1)}$ is the lowest gate resistance and $V_{OS(i=1)}$ is the corresponding voltage overshoot).

Figure 6-17 (a) and Figure 6-18 (a) demonstrate the contour distribution of V_{OS} (i.e. *di/dt*) controllability of Module-A and *dv/dt* controllability of Module-B. It can be found that both modules present higher controllability when they are operating at low-V_{DC} and high-I_L conditions, which confirms to the theoretical analysis and simulation results in previous sections. Note that the *dv/dt* stage of Module-A and *di/dt* stage of Module-B are not plotted since the former shows effective control under all conditions and the latter shows a total loss of control under all conditions.

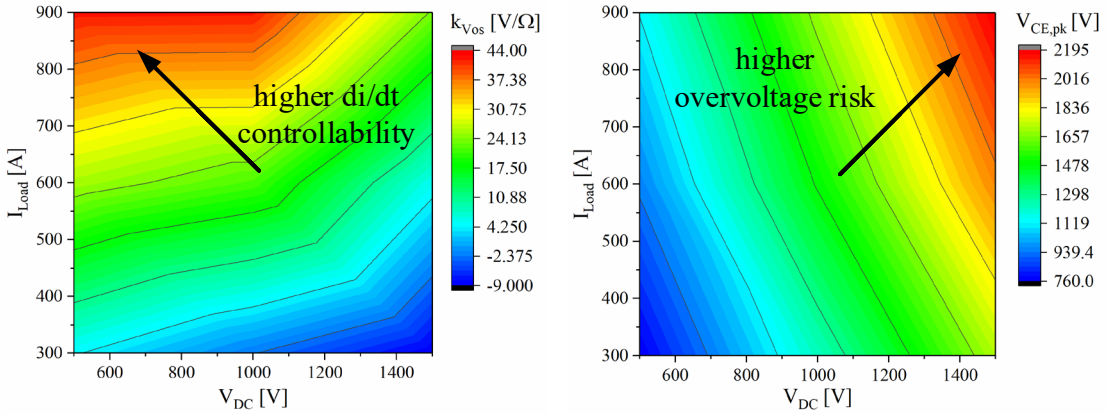
6.6.1 Discussion of Module-A

Module-A has effective gate control over *dv/dt*, but the defective control over *di/dt* is observed under some conditions. In Figure 6-17 (b), the contour distribution of the peak voltage $V_{CE,pk}$ of Module-A during its turn-off is given with respect to various load conditions. It can be seen that the higher V_{DC} and I_L, the higher $V_{CE,pk}$ that Module-A will be exposed to, thus causing the reduction in the voltage safety margin.

Conventional gate driver is currently a prevailing option for high-power IGBT modules, which adopts constant gate resistance with pre-set values. To avoid overvoltage in all operating conditions, larger turn-off resistor R_{G_ext} is always chosen by design engineers

following a conservative philosophy. This will inevitably cause extra switching loss, delays and low frequency switching operations, especially when IGBT modules have weaker V_{OS} (i.e. *di/dt*) controllability.

Therefore, to make the best use of the high V_{OS} (i.e. *di/dt*) controllability in the suppression of the over-voltage stress, modifications in the chip design can be considered by manufacturers. For example, to slightly reduce the on-state charge carrier distribution in drift layer near the emitter of IGBT cell. The objective is to improve the *di/dt* controllability at the high-risk conditions as indicated in Figure 6-17 (b) rather than all operating conditions.

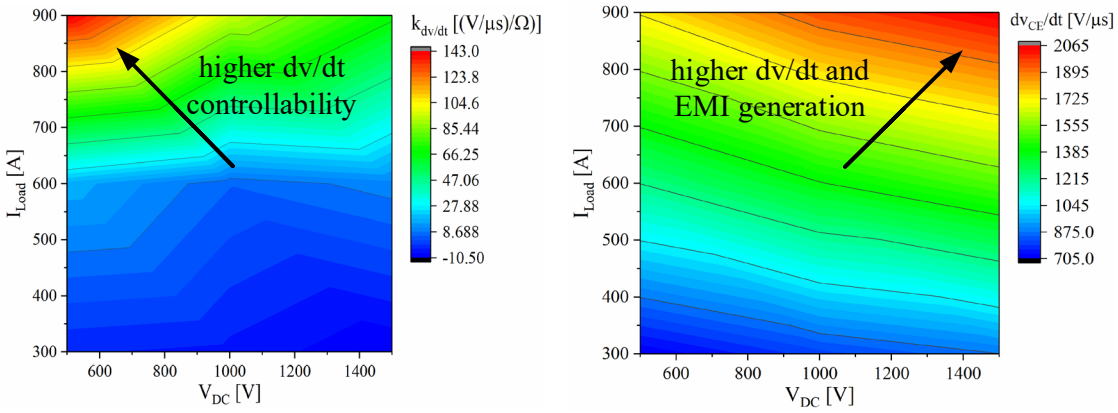


(a) *(b)*

Figure 6-17: Contour distribution of Module-A at various load conditions (a) V_{OS} controllability; (b) $V_{CE,pk}$ at R_{G_ext}= 1.65 Ω.

6.6.2 Discussion of Module-B

Module-B presents an earlier arrival of defective gate control during *dv/dt* stage under some conditions, and an entirely loss of control over *di/dt*. In Figure 6-18 (b), the contour distribution of the *dv/dt* values of Module-B during its turn-off is given with respect to various load conditions. It clearly shows the higher *dv/dt* occurs at higher V_{DC} and I_L. For applications, this will increase difficulties to address intra- and inter-equipment EMI issues. A common design option to suppress high *dv/dt* is to apply larger turn-off R_{G_ext}. This can inevitably cause increased turn-off losses and turn-off delay time, which is even more obvious for IGBT modules with weaker *dv/dt* controllability. Therefore, it is better to improve the *dv/dt* controllability at the higher *dv/dt* conditions as indicated in Figure 6-18 (b) rather than all operating conditions.



(a) *(b)*

Figure 6-18: Contour distribution of Module-B at various load conditions (a) dv/dt controllability; (b) dv/dt at R_{G_ext}=1.65Ω.

6.7 Summary of Chapter 6

The *di/dt* and *dv/dt* rates are important to HV-IGBT modules' application, however, their defective controllability manifests during turn-off transitions for both the trench-gate and the planar-gate designs. The impact factors of operating conditions on the device controllability have been investigated and experimentally examined. It can be concluded that the most challenging conditions regarding their controllability take place at higher bus voltage, lower load current, and lower gate resistance. Thereafter, finding the occurrence time of MTP at a targeted worst condition enables the controllability assessment for IGBT to be completed by fewer dynamic tests. This avoids exhaustive tests under massive number of operating conditions, as well as data post-processing. Moreover, the gate-emitter voltage measured at the module auxiliary terminals can be severely distorted when the gate resistance ratio *r* is high, which can be calibrated by the proposed method. On the basis of tested modules, it is suggested to take the device controllability into account when designing the IGBT chip to benefit its application in converter systems.

CHAPTER 7

Conclusions

7.1 Conclusions

The increasing demands and expectations in high-reliability, high-efficiency, and less fabrication and maintenance costs in the high-power converter system have established the motivation of this research work. To meet these rigorous requirements, solutions can be found at the heart of the high-power converter: the IGBT module and its peripheral gate driver circuit. The objectives set for this work covered several important topics, including the device behavioural modelling, the experimental test platform, the electronic circuit design of gate driver, and performance evaluation method.

To practically characterise the high-power IGBT modules and validate the control effectiveness of gate driving circuit, a DPT platform with testing range covering up to 2400V/1500A operating condition and the maximum chip temperature of device has been built. Furthermore, with the designed computer-aided software applied to the control and the data post-processing, both efficiency and accuracy of the test platform can be improved, and the workload of researcher or operator can be effectively reduced.

With the increment in power rating of the DUT, the testing condition range is expanded in both voltage and current, which could significantly boost the cost in system construction. A generalised design procedure is proposed for the bank capacitor and load inductor selection, to achieve both high testing capability and cost effectiveness. The generalised design method could potentially be applied in the platform design for other testing requirements or devices.

Additionally, auxiliary hardware and computer-aided software are tailored for the platform. (1) Two separated heat-plates were assembled on the platform beneath IGBT modules to enable their temperature control up to maximum rating separately. (2) The

PCB-mounted relays are designed to execute the charging and discharging manners of test system, which provides a space-saving solution for the high-voltage DPT rig. (3) The LabVIEW program implemented in controller provides a user-friendly UI for test rig remote control from a computer, which simplifies the test procedure and reduces the chance of touching the equipment. (4) Programmed MATLAB code is applied to analyse experimental results and extract characterisation features in an efficient way. Moreover, it provides standardised calculation for more accurate analysis. (5) Measuring techniques including the implementing skill, the bandwidth, the random noise, and the de-skew calibration are all carefully considered to achieve more accurate measurement. It has been revealed that, despite the switching speed of high-power module is much slower than WBG devices, a 30ns dis-alignment in current and voltage probes can still generate more than 5% error in switching loss calculation. The influence of random noise in high-voltage and high-current measurements is also amplified as the targeted signal need to be attenuated in measurement system.

A comprehensive analytical model to describe the dynamic characteristics of IGBT module was derived. The model considers not only the control effects of the conventional voltage-source driving method but also the current-source driving concept. From the model derived, it was possible to determine the control impact of all potential parameters that can be implemented in advanced active driving techniques (i.e. gate resistance, gate voltage, and gate current).

To date, there has been a little consideration of the comparison among these candidate driving parameters. A comparative study on candidate driving parameters has been done. Among them, the gate current been found the most promising driving parameter. For active gate voltage control method, the dynamic range of gate voltage supply has restricted limitations. For the current-source driver, it has unique features. Firstly, the current-source driving can decouple the influences of load current on Miller voltage and *dv/dt* during switching. Secondly, controlling the gate current is the most direct method to control the gate charge, which determines the switching transient characteristics. By implementing current to charge/discharge the gate of IGBT, either at fixed or dynamically changed current values, the gate charge information can be easily obtained by controller

due to the charging/discharging time is already known. This feature could be used to realise advanced control algorithm.

After selecting the target driving parameter, a new driving circuit topology of current-source-based array is proposed to drive the high-power IGBT module. It is advantageous in control flexibility, low-cost, and ease of integration. Each current source in the array can provide large current injection and sink with fast dynamic performance. In the proposed intelligent gate driver concept, the active driving circuit which enables adjustment of gate driving pattern is a key part. The experimental results show that by implementing the proposed active current-source gate driver, the turn-on/off transient process can be controlled to achieve reduced switching losses, electrical stresses and delay time compared with the conventional method.

The controllability of high-power IGBT modules needs more attention, as it restricts the module performance in conventional application and could also prevent the merits brought by advanced driving techniques. The defective *di/dt* and *dv/dt* controllability during turn-off transition can be found in both the trench-gate and the planar-gate designs. The impact factors of operating conditions on the device controllability have been investigated and experimentally examined. It can be concluded that the most challenging conditions regarding their controllability take place at higher bus voltage, lower load current, and lower gate resistance. Thereafter, finding the occurrence time of MTP at a targeted worst condition enables the controllability assessment for IGBT to be completed by fewer dynamic tests. This avoids exhaustive tests under massive number of operating conditions, as well as data post-processing. Moreover, the gate-emitter voltage measured at the module auxiliary terminals can be severely distorted when the gate resistance ratio r is high, which can be calibrated by the proposed method. On the basis of tested modules, it is suggested to take the device controllability into account when designing the IGBT chip to benefit its application in converter systems.

7.2 Future Work

For the designed test platform, the LabVIEW program implemented in National Instruments cDAQ controller can be further developed with more functions. It can be

used to communicate with more instruments, including oscilloscope and programmable voltage supply with the general purpose interface bus (GPIB) interface, for remote and easy control. Intelligent control algorithm based on the information sensed by the gate driver can be developed, thus the driving pattern can be controlled for the switching transient characteristics optimisation under more complicated operating conditions and tackling long-term health status issues of power devices. The transient uncontrollability in *di/dt* and *dv/dt* in high-power IGBT module should be taken into account in semiconductor design. The investigation in the thesis is limited to room temperature. However, the junction temperature influences semiconductor characters including the switching rates, the switching delay times, the threshold and Miller voltages, and even the internal gate resistance, which is a challenging topic that needs further research.

APPENDIX A

Simulation Circuits

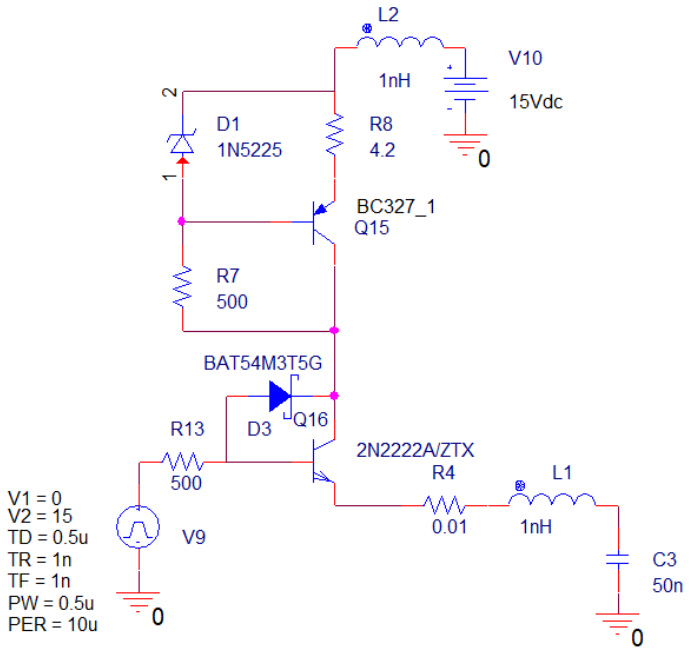


Figure A - 1: Simulation circuit for ZCS evaluation.

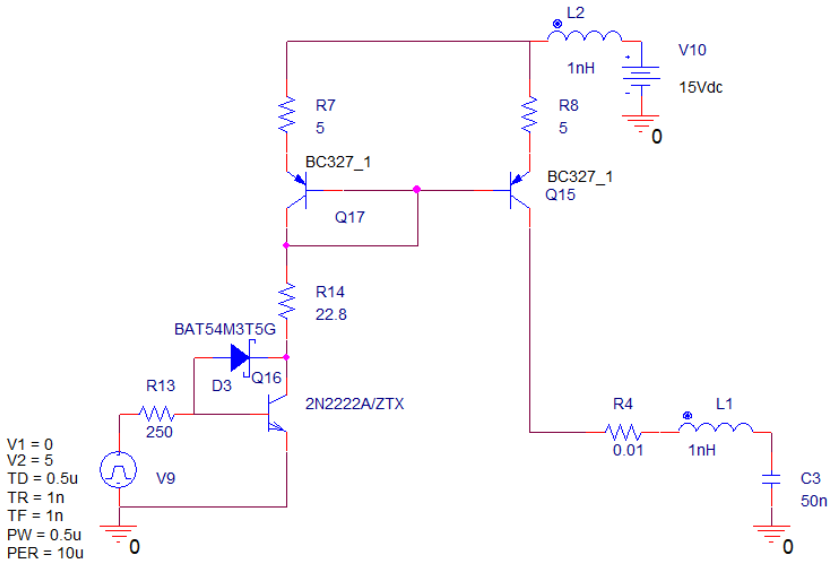


Figure A - 2: Simulation circuit for MCS evaluation.

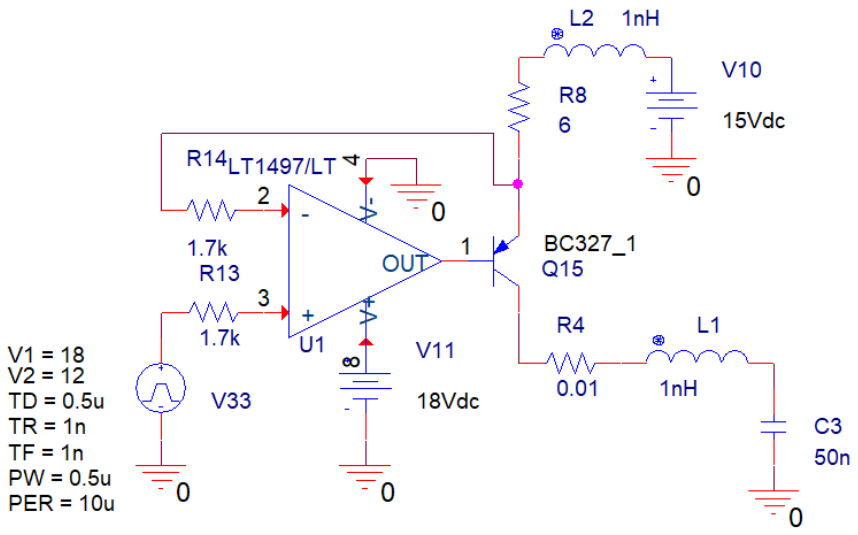


Figure A - 3: Simulation circuit for OCS evaluation.

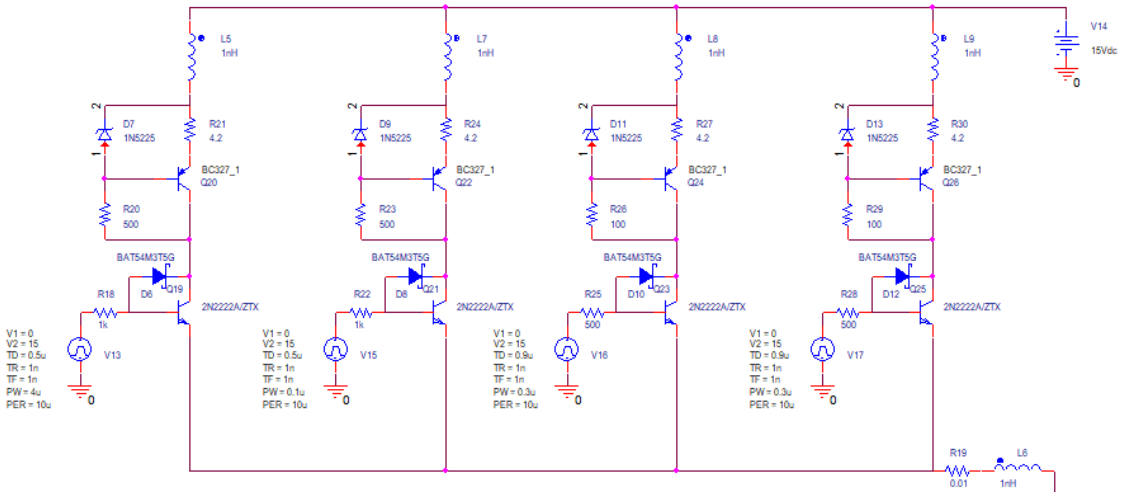


Figure A - 4: Turn-on array of ZCS circuits.

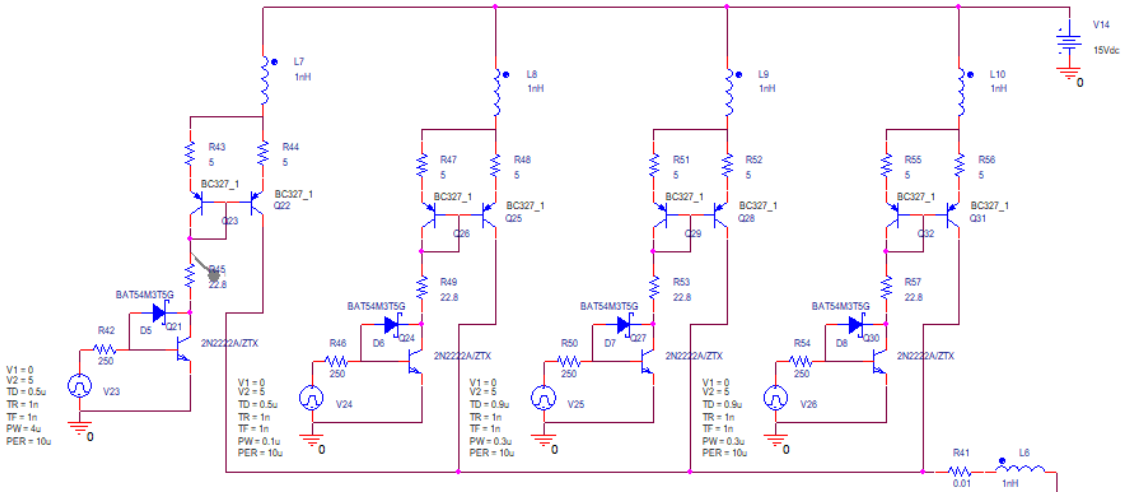


Figure A - 5: Turn-on array of MCS circuits.

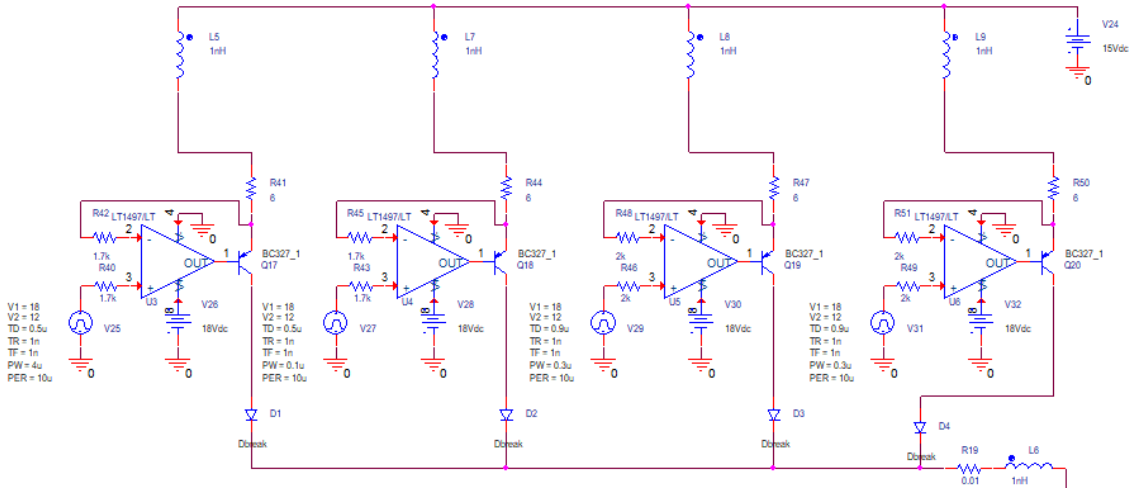
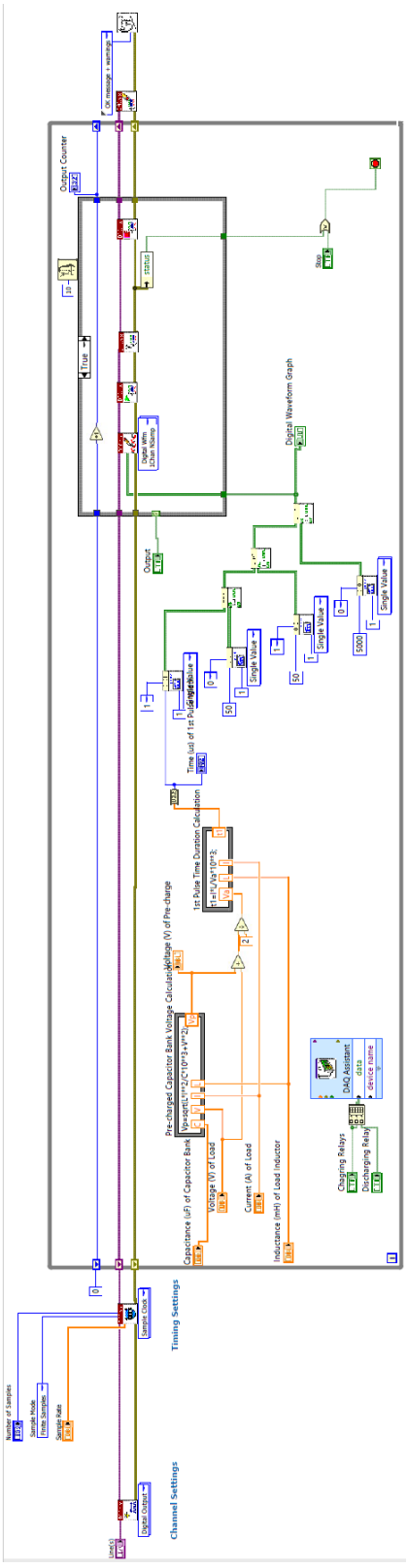


Figure A - 6: Turn-on array of OCS circuits.

APPENDIX B

LabVIEW User Interface Code



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