Analytical Model for Predicting the Junction Temperature of Chips Considering the Internal Electrothermal Coupling inside Silicon Carbide MOSFET modules

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Abstract: Due to their excellent characteristics, silicon carbide MOSFET modules are expected to have broad application prospects in various types of power conversion equipment in the future. Accurate prediction of the internal chip junction temperature of SiC module is of great value for the usage of the modules in the power conversion equipment. In this paper, taking the electrothermal coupling process and the thermal characteristics of the chips into consideration, the power loss model under unipolar and bipolar SPWM control was developed. A star-shaped equivalent thermal network model based on virtual temperature was established. And an analytical junction temperature predicting model was proposed. To obtain the temperature dependency of static and dynamic parameters for the models, power device analyzer was used and double pulse test bench was established. For the purpose of validating the effectiveness and accuracy of the above models, the finite element method was used to calculate the junction temperature of a commercial 1200V/300A full silicon carbide module under different working conditions. The results show that the relative error is very small and the proposed model are effective.

1. Introduction

Compared with silicon material, silicon carbide (SiC) material has higher band gap, greater breakdown field strength and better thermal conducting and thermal stability characteristics [1-4]. The features give SiC power devices the ability to operate at higher frequency, higher temperature and lower losses among other outstanding performance advantages [5-6]. At present, the full SiC module consisting of SiC MOSFET and SiC SBD has gradually become well known. And that has a very broad application prospect in converter applications such as power electronic transformers in the future [7-8]. However, converters face reliability challenges. And one of the major causes for converter damage is the overheating failure of the power module internal chips. The thermal failure of the module is a complex electrothermal coupling process. The static characteristics of chips, the power loss and the temperature are coupled through the power loss, the thermal characteristics of chip parameters and the thermal resistance network. Therefore, in order to make full use of the excellent performance of SiC module and make it working safely and stably in complex environments, it is necessary to comprehensively analyze the electrothermal coupling process in the module. Therefore, it's important and meaningful to obtain the thermal characteristics of chip parameters, power loss model, thermal network and temperature predicting method.

Temperature has an influence on the electrical parameters through the thermal characteristics of chip parameters. Some researchers have done relative work about this field on SiC chips. Reference [9] compared the leakage current, threshold voltage and on-state voltage drop of SiC MOSFET from room temperature to 250 °C temperature range. The literature [10] comparatively analyzed the various static characteristics of temperature for SiC MOSFET and Si IGBT. Some researchers have analyzed the temperature dependency of a dynamic parameter, dI/dt, of SiC MOSFET [11]. The temperature-dependent characterization of saturation current, output characteristics and antiparallel diode of 10 kV SiC MOSFET has also been studied by simulation [12]. However, it has not been further studied in literatures that how temperature changes can have an indirect effect on device or chip losses through different parameters.

Power modules generate heat when they work. Most heat comes from the power loss of chips. Some literatures offer some calculating method or test results for power loss of SiC power devices. Reference [13] proposed a simplified loss analysis method for SiC MOSFET inverter with the datasheet. Using testbench based on boost converter or isolated DC/DC converters, the switching energy under different working conditions were measured in reference [14-15]. In literature [16], an analytical loss model for power converters with SiC MOSFET and SiC SBD pair was proposed. The influence of load current and gate resistance was considered but the temperature effect was not mentioned.

The thermal resistance network plays a very important role during the electrothermal coupling inside power devices. And many researchers utilize thermal resistance network to predict the temperature of power module or chips. Reference [17] predicted the mean junction temperature of IGBT module with thermal network model. Reference [18] designed a simplified dynamical thermal model for converters. The temperature and lifetime of press-pack IGBT were predicted using the model. Some researchers thoroughly studied the influence of mutual thermal impedance and improved the thermal network used for IGBT junction temperature prediction [19]. Considering the effects of base plate solder fatigue, literature [20] proposed an improved thermal network model for IGBT modules. In reference [21], researchers modified the Cauer-type thermal network model

of an IGBT by considering error caused by cross heat transmission time delay.

There is lots of excellent work about the thermal characteristics of chip parameters, power loss calculation and thermal network for power devices. But almost no one has done a close-loop analysis and offered analytical temperature predicting model in the electrothermal coupling process of SiC module. In this paper, the power loss model of SiC MOSFET and SBD under the unipolar and bipolar SPWM control is developed. Then, the thermal network model of the SiC power module based on virtual temperature is proposed. And the thermal network is extracted by the conjugate gradient method in this paper. On the basis of the power loss model and the thermal network model, an analytical chip junction temperature predicting model for the SiC module taking the close-loop electrothermal coupling into consideration is established. The model can be used to analyze the analytical relationship between different parameters and the junction temperature of the chip. Moreover, the power device analyzer and the double pulse test platform are used to test the static and dynamic parameters of SiC MOSFET and SiC SBD at different temperatures. Finally, a 3D model of SiC module is built, on which basis the accuracy of the thermal network model and the temperature predicting model is verified by comparing the model calculation results with the finite element simulation results under different working conditions.

2. Modelling

2.1. Power Loss Calculation

In order to analyze the electro-thermal coupling and obtain the temperature distribution of SiC modules used for converters, it is necessary to calculate power losses of chips in the module accurately under practical converter working conditions. The power loss of the SiC module mainly comes from the losses generated by SiC MOSFET and SiC SBD during on state and switching processes. Since the reverse recovery time is very short, the switching loss of SiC SBD is negligible.

Each SiC MOSFET and SiC SBD chip inside the module is an independent heat source, so the MOSFET chip loss P_{mos_tot} and SBD chip loss P_{sbd_tot} in the module can be calculated separately, which can be expressed as (1) and (2).

$$P_{mos\_tot} = P_{con\_mos} + P_{swi} \tag{1}$$

$$P_{sbd\_tot} = P_{con\_sbd} \tag{2}$$

Where, P_{con_mos} and P_{swi} are respectively the conduction and the switching losses of each SiC MOSFET chip, and P_{con_sbd} is the conduction loss of each SiC SBD chip.

2.1.1. Conduction Loss

Sinusoidal pulse width modulation (SPWM) method is widely used in the controlling of converters. Based on equivalent area compensation, SPWM control methods can be divided into unipolar and bipolar SPWM methods according to the polarity of the carrier within half signal wave cycle. Due to the adaption of SPWM modulation method, load current i_L is approximately sinusoidal and can be expressed as (3).

$$i_L = I_m \sin \omega t \tag{3}$$

In (3), I_m is the peak load current, ω is the angular frequency of the current wave.

To improve the effective value of the load current with SPWM controlling method, the harmonic injection pulse width modulation (HIPWM) is most commonly used in practical applications. By injecting a certain proportion of the third harmonic into the sinusoidal wave, the modulated wave is manifested as saddle-shaped, resulting in a reduction in the amplitude of the modulated wave. Taking the A phase as an example, the modulation wave expression should be as shown in (4) [22].

$$v_A = \frac{2}{\sqrt{3}} V_0 (\sin \omega t + \frac{1}{6} \sin 3\omega t) \tag{4}$$

Where, v_A is the A-phase voltage, V_0 is the reference voltage value, ω is the angular frequency of the current wave.

Using the regular sampling method [22-23] for HIPWM modulation and considering the phase angle θ, the following expression (5) can be obtained.

$$\frac{\delta}{T_C} = \frac{1}{2} + \frac{\sqrt{3}}{3} M \sin(\omega t + \theta) + \frac{\sqrt{3}}{18} M \sin(3(\omega t + \theta)) \tag{5}$$

Where, T_C is the carrier period, M is the degree of modulation, $0 \le M < 1$, δ represents the turn-on time in a period.

2.1.1.1. Conduction Loss of SiC MOSFET

In the conduction state, the on-state voltage v_{DS} of SiC MOSFET can be expressed as a function of its on-resistance R_{DS} and on-current i_L (6). The relationship between on-resistance R_{DS} and chip junction temperature T_j can be approximately expressed as a linear function (7) [24].

$$v_{DS} = R_{DS} i_L \tag{6}$$

$$R_{DS} = a_{rds} T_j + b_{rds} \tag{7}$$

Where, a_{rds} is the temperature coefficient of R_{DS}, and b_{rds} is the value of R_{DS} when T_j=0.

With unipolar PWM modulation, the SiC MOSFET operates only in half a cycle. So according to (3)(5)(6)(7), the conduction loss can be expressed as (8).

$$\begin{aligned} P_{un\_con\_mos} &= \frac{1}{T} \int_0^{\frac{T}{2}} v_{DS} i_L \frac{\delta}{T_C} \mathrm{d}t \\ &= \left(a_{rds} T_j + b_{rds}\right) I_m^2 \left(\frac{1}{8} + \frac{2\sqrt{3}}{9\pi} M \cos\theta - \frac{\sqrt{3}}{135\pi} M \cos 3\theta\right) \end{aligned} \tag{8}$$

With bipolar PWM modulation, the upper and lower arms of the SiC MOSFET are alternately switched on, and the device operates in the full cycle. Similarly, the conduction loss can be expressed as follows.

$$\begin{aligned} P_{bi\_con\_mos} &= \frac{1}{T} \int_0^{T} v_{DS} i_L \frac{\delta}{T_C} \mathrm{d}t \\ &= \frac{1}{4} I_m^2 \left(a_{rds} T_j + b_{rds}\right) \end{aligned} \tag{9}$$

2.1.1.2. Conduction Loss of SiC SBD

The forward voltage drop v_F of the SiC SBD can be expressed as the sum of saturation voltage drop V_{FS} and the forward conduction resistance R_F. V_{FS} and R_F can also be seen as a linear function of T_j [25].

$$v_F = V_{FS} + R_F i_L \quad (10)$$

$$V_{FS} = a_{vfs} T_j + b_{vfs} \quad (11)$$

$$R_F = a_{rf} T_j + b_{rf} \quad (12)$$

Where, a_{vfs} and a_{rf} are the temperature coefficient of V_{FS} and R_F, while b_{vfs} and b_{rf} are the value of V_{FS} and R_F respectively when T_j=0.

In the SiC module, the SiC SBD mainly acts as the freewheeling diode for the SiC MOSFET, and switches on when SiC MOSFET switches off, so the SiC SBD conduction time is T_C-δ in each carrier signal period.

In the case of unipolar SPWM modulation, the conduction loss of SiC SBD can be expressed by (3) (5) (10) (11) (12) as follows.

$$\begin{aligned} P_{un\_con\_sbd} &= \frac{1}{T}\int_0^{\frac{T}{2}} v_F i_L \frac{T_C - \delta}{T_C} dt \\ &= I_m \left(a_{vfs} T_j + b_{vfs}\right)\left(\frac{1}{2\pi} - \frac{\sqrt{3}}{12} M \cos\theta\right) \\ &+ I_m^2 \left(a_{rf} T_j + b_{rf}\right)\left(\frac{1}{8} - \frac{2\sqrt{3}}{9\pi} M \cos\theta + \frac{\sqrt{3}}{135\pi} M \cos 3\theta\right) \end{aligned} \quad (13)$$

Similarly, in a converter using bipolar SPWM modulation, the conduction loss of a SiC SBD can be expressed as (14).

$$P_{bi\_con\_sbd} = \frac{1}{T}\int_0^T v_F i_L \frac{T_C - \delta}{T_C} dt = \frac{1}{4} I_m^2 \left(a_{rf} T_j + b_{rf}\right) \quad (14)$$

2.1.2. Switching Loss

For SiC SBD, the switching loss is usually negligible due to its extremely fast switching speed and almost zero reverse recovery time. Moreover, the junction temperature almost has no influence on the switching characteristics of SiC SBD. Therefore, during the switching process of the SiC MOSFET power module, only the switching loss of the SiC MOSFET performs an important role.

During the turn-on period of the SiC MOSFET, the current rises first and then the voltage drops. During the turn-off period, the voltage rises first and then the current falls. The transient changing of the voltage and current with time is approximately linearly. The switching loss of SiC MOSFET at a certain voltage and current level can be approximately considered to be inversely proportional to the switching speed and proportional to the sum of turn-on and turn-off time. The turn-on time t_{on} and turn-off time t_{off} of the SiC MOSFET can be expressed as follows [26].

$$t_{on} = R_G C_{iss} \ln\left(\frac{V_{GH}}{V_{GH} - V_{th} - \sqrt{i_L / G_F}}\right) + R_G C_{GD} \frac{V_L}{V_{GH} - V_{mil}} \quad (15)$$

$$t_{off} = R_G C_{GD} \frac{V_L}{V_{mil}} + R_G C_{iss} \ln\left(\frac{V_{mil}}{V_{th}}\right) \quad (16)$$

Where, f_s is the switching frequency, V_{GH}, V_L and V_{mil} are the driving supply voltage, the DC bus voltage, and the gate-source Miller platform voltage respectively. R_G, C_{iss} and C_{GD} are the gate resistance, input capacitance and miller capacitance respectively. Transconductance coefficient G_F and threshold voltage V_{th} are expressed as (17).

$$i_D = G_F (v_{GS} - V_{th})^2 \quad (17)$$

Where, i_D is the drain current and v_{GS} is the gate-source voltage.

According to reference [27], turn-on and turn-off switching energy can respectively be expressed as the proportional function of turn-on and turn-off time. And both the turn-on and turn-off energy are the proportional function of bus voltage V_{DD} and peak load current I_m. The switching loss of SiC MOSFET under different parameter conditions can be expressed as (18).

$$P_{swi} = f_s \left(E_{on0} \frac{t_{on}}{t_{on0}} + E_{off0} \frac{t_{off}}{t_{off0}}\right) \frac{V_{DD} \cdot I_m}{V_{DD0} \cdot I_{m0}} \quad (18)$$

Where, E_{on0} and E_{off0} respectively represent the turn-on and turn-off energy of SiC MOSFET under an initial state, t_{on0} and t_{off0} are the turn-on time and turn-off time of the SiC MOSFET in an initial state respectively. V_{DD0} and I_{m0} are the initial bus voltage and peak load current.

2.2. Thermal Network Model

In the SiC MOSFET module, all SiC MOSFET chips and SiC SBD chips are heat sources, so the temperature rise of a chip is related not only to its own heat generation and heat dissipation, but also to the heat transfer from other heat sources. When the temperature reaches a steady state, all of the chip heat sources in the module can be connected with a complex thermal resistance network. For a device with n chips, the thermal network model used to represent the steady-state thermal resistance network model is shown in Fig.1, and the mutual thermal resistance network among the chips can be regarded as an n-terminal full mesh thermal network (FTN). It can be seen that as the number of chips increases, the number of thermal resistances in the thermal network n_R can be expressed as (19).

$$n_R = \frac{n(n+1)}{2} \quad (19)$$

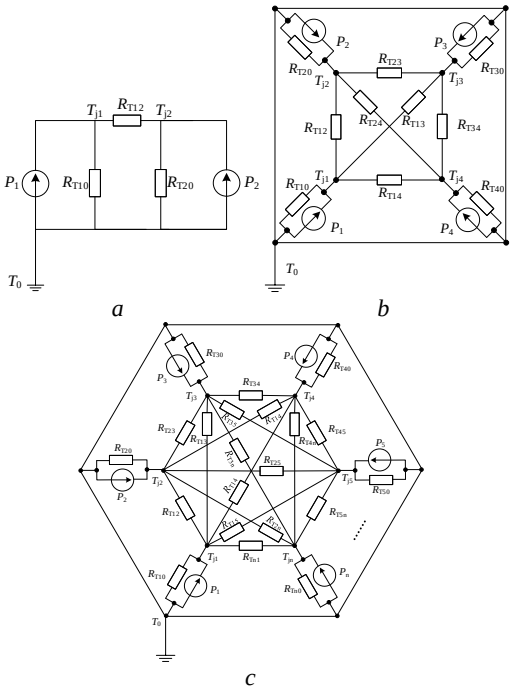

Fig. 1. *Multi-chip steady-state thermal resistance network* ***(a)*** 2-chip network, ***(b)*** 4-chip network, ***(c)*** n-chip network

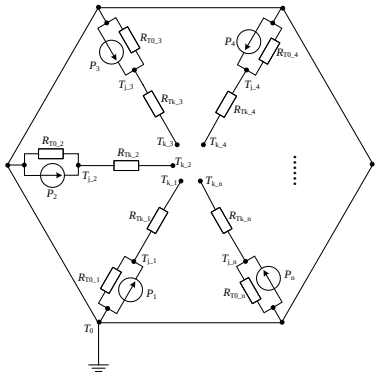

Fig. 2. *Multi-chip equivalent thermal resistance network*

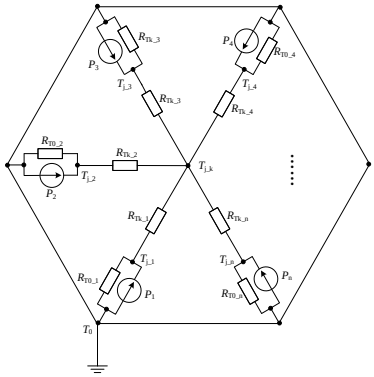

Fig. 3. *Star-shaped multi-chip steady-state thermal network model based on virtual temperature method*

The n-chip FTN shown in Fig. 1. (c) is able to be equivalent to a thermal network with virtual temperatures as shown in Fig. 2. All the virtual temperatures from T_{k_1} to T_{k_n} is not fixed. They are affected by the thermal resistances R_{Tk_1} to R_{Tk_n} and different chip junction temperature. The positive direction of the power loss in every branch is from the virtual temperature to the junction temperature. The Fig. 2. can be transformed to a star-shaped thermal network (STN) as shown in Fig.3. when the following two prerequisites are met. (a) The virtual temperature values in different branches are the same. (b) The sum of all the power losses of the n branches is zero. The heat transfer among the chips is equivalent to that between the chips and the isothermal surface of the virtual temperature. The virtual temperature T_k does not have a fixed value here and the value of T_k varies with different working conditions for a power module. By introducing virtual temperature T_k, the n-terminal full mesh thermal resistance network can be transformed into an n-terminal star thermal network and the number of thermal resistances in the network can be reduced to $2n$. When the number of chips is large, the thermal resistance extraction efficiency can be significantly improved and the temperature predicting model can be simplified.

In order to meet the mentioned prerequisites and obtain the values of thermal resistances that in STN, a thermal network extraction method based on the conjugate gradient method is proposed. This method is used to optimize values of the thermal resistances to minimize the difference among the virtual temperatures from T_{k_1} to T_{k_n}. The thermal network will be equivalent to the STN when the difference is small enough. For making the equivalent STN can work well in more conditions, m groups of simulating or experimental results under different working conditions are requested. The indicator S as shown in (20) is introduced to measure the comprehensive difference among virtual temperatures of the n branches in the m groups of results.

$$S = \frac{1}{m(n-1)} \sum_{i=1}^{m} \sum_{j=1}^{n} \left(T_{k\_ij} - \overline{T}_{k\_i} \right)^2 \qquad (20)$$

Where, T_{k_ij} is the virtual temperature value in the j branch of No.i experiment or simulation, and $\overline{T}_{k\_i}$ is the average virtual temperature for No.i experiment or simulation.

For each branch, the virtual temperature T_{k_ij} can be expressed as shown in (21). Since the power sum of n branches is 0, the relational expression can be listed as shown in (22).

$$T_{k\_ij} = \left(\frac{T_{j\_ij}}{R_{T0\_j}} - P_{ij} \right) R_{Tk\_j} + T_{j\_ij} \qquad (21)$$

$$\sum_{j=1}^{n} \frac{T_{k\_ij} - T_{j\_ij}}{R_{Tk\_j}} = 0 \qquad (22)$$

Where, T_{j_ij} and P_{ij} are the junction temperature and power loss of the j_{th} chip in the i_{th} condition respectively. R_{T0_j} and R_{Tk_j} are the equivalent heat dissipation resistance and equivalent heat transfer resistance of the j_{th} chip.

The conjugate gradient method takes the negative gradient direction of the current point and conjugates it with the previous search direction, generating the search direction of the current point. When the problem variable has a large number of dimensions, the conjugate gradient method is a very effective nonlinear optimization method [28]. Set the virtual temperature comprehensive difference coefficient S as the optimized objective function, and solve the thermal resistance network when S is minimum as well as the equations (21) and (22) are met. If the result S is sufficiently small, it can be verified that the thermal network simplification approximation of Fig.1(c) to Fig.3 is established.

The famous FR conjugate gradient method and Goldstein line search are used here for minimize the S indicator. According to reference [29], the FR conjugate gradient method converges globally under the Goldstein line search conditions. Therefore, the thermal network model proposed in this manuscript is convergent.

2.3. Electro-thermal Coupled SiC Chip Temperature Predicting Model

2.3.1. Temperature Predicting Model

The power loss model has been established in this paper. It can be seen from the model that in any case, both of the switching loss and conduction loss of SiC chips are linear with the junction temperature. So, it can be concluded that the total loss of every chip is a linear function of the chip temperature, which can be expressed as (23).

$$P_{tot\_i} = a_i T_{j\_i} + b_i \qquad (23)$$

Where, T_{j_i} and P_{tot_i} are the junction temperature and total loss of the i_{th} chip respectively. And a_i and b_i represent the temperature coefficient of the total loss of the chip and the loss when temperature equals to 0.

If the thermal network of the module is extracted with through the optimization, the thermal network is transformed to the STN shown in Fig.3. And the expression of T_{j_i} could be expressed as (24).

$$T_{j\_i} = T_{j\_k}\frac{\dfrac{1}{R_{Tk\_i}}}{\dfrac{1}{R_{Tk\_i}}+\dfrac{1}{R_{T0\_i}}-a_i} + \frac{\dfrac{T_0}{R_{T0\_i}}+b_i}{\dfrac{1}{R_{Tk\_i}}+\dfrac{1}{R_{T0\_i}}-a_i} \tag{24}$$

According to equations (23) and (24), the following matrix equation can be deduced.

$$\begin{bmatrix} T_{j\_1} \\ T_{j\_2} \\ \vdots \\ T_{j\_n} \\ T_{j\_k} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \cdots & 0 & c_{1k} \\ 0 & 0 & \cdots & 0 & c_{2k} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & 0 & c_{nk} \\ c_{k1} & c_{k2} & \cdots & c_{k6} & 0 \end{bmatrix} \begin{bmatrix} T_{j\_1} \\ T_{j\_2} \\ \vdots \\ T_{j\_n} \\ T_{j\_k} \end{bmatrix} + \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_n \\ 0 \end{bmatrix} \tag{25}$$

Where, c_{ki}, c_{ik} and d_i are functions of R_{Tk_i}, R_{T0_i}, a_i and b_i. They can be respectively represented by the following equations.

$$c_{ki} = \frac{\dfrac{1}{R_{Tk\_i}}}{\displaystyle\sum_{i=1}^{n}\frac{1}{R_{Tk\_i}}} \tag{26}$$

$$c_{ik} = \frac{\dfrac{1}{R_{Tk\_i}}}{\dfrac{1}{R_{Tk\_i}}+\dfrac{1}{R_{T0\_i}}-a_i} \tag{27}$$

$$d_i = \frac{\dfrac{T_0}{R_{T0\_i}}+b_i}{\dfrac{1}{R_{Tk\_i}}+\dfrac{1}{R_{T0\_i}}-a_i} \tag{28}$$

On the basis of equation (25), the analytical junction temperature predicting model of each chip can be derived as (29).

$$\begin{bmatrix} T_{j\_1} \\ T_{j\_2} \\ \vdots \\ T_{j\_n} \end{bmatrix} = \frac{1}{1-\displaystyle\sum_{p=1}^{n} c_{pk}c_{kp}} \begin{bmatrix} 1-\displaystyle\sum_{p=2}^{n} c_{pk}c_{kp} & c_{k2}c_{1k} & c_{k3}c_{1k} & \cdots & c_{kn}c_{1k} \\ c_{k1}c_{2k} & 1-\displaystyle\sum_{\substack{p=1 \\ p\neq 2}}^{n} c_{pk}c_{kp} & c_{k3}c_{1k} & \cdots & c_{kn}c_{1k} \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ c_{k1}c_{nk} & c_{k2}c_{nk} & \cdots & c_{kn-1}c_{nk} & 1-\displaystyle\sum_{p=2}^{n-1} c_{pk}c_{kp} \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_n \end{bmatrix} \tag{29}$$

2.3.2. Influence of Different Parameters on Chip Temperature

Due to the analytical expression obtained from the temperature predicting model is complicated. It is difficult to directly find the law of the influence of different parameters on the chip temperature. However, after simplification, the function of the junction temperature affected by an influencing factor x_i can be separately obtained.

When considering the influence of the temperature characteristics of chip j on the junction temperature of chip i, parameters only related to other chip parameters and converter operating parameters can be regarded as constants. Therefore, the relationship of the junction temperature and the temperature characteristics of i_{th} chip can be simplified to (30).

$$T_{j\_i} = s_1 + \frac{s_2 b_j + s_3}{a_j + s_4} \quad , \quad i, j = 1, 2, \ldots, n \tag{30}$$

Where, s_1, s_2, s_3 and s_4 are parameters independent of temperature coefficient of the j_{th} chip.

As for b_{rds}, b_{rf}, b_{vfs}, E_{on} and E_{off} of the j_{th} chip, these parameters are only linearly related to b_j. Hence, the relationship between T_{j_i} and these parameters is also linear, and the predicted junction temperature can be expressed as (31).

$$T_{j\_i}(x_j) = q_1 x_j + q_2 \quad , \quad i, j = 1, 2, \ldots, n \tag{31}$$

Meanwhile, a_{rds}, a_{rf} and a_{vfs} of the j_{th} chip are only linearly related to a_j. T_{j_i} can be rewritten as (32).

$$T_{j\_i}(x_j) = \frac{q_3}{x_j + q_1} + q_2 \quad , \quad i, j = 1, 2, \ldots, n \tag{32}$$

It can be seen from (32) that T_{j_i} has a nonlinear relationship with a_{rds}, a_{rf} and a_{vfs}.

Since the switching loss of all SiC MOSFET chips is proportional to the switching frequency f_s and the switching loss of the SiC SBD chip is negligible, the switching frequency f_s can be considered to have a linear relationship with the b_i of each chip. After simplification. The relationship between the temperature of the i_{th} chip and the switching frequency can be expressed as (33).

$$T_{j\_i}(f_s) = q_1 f_s + q_2 \tag{33}$$

Where, q_1, q_2 and q_3 are independent of parameters of the j_{th} chip.

3. Extraction of Electrical Parameters

3.1. Static Parameter Extraction

In this paper, commercial SiC MOSFET and SBD from an internationally renowned manufacturer are selected for testing. The temperature is controlled and measured by an auxiliary heat source and a thermal resistor respectively. Static parameters including R_{DS} of SiC MOSFET together with V_{FS} and R_F of SiC SBD under different temperatures are measured by power device analyzer and curve tracer. The static parameters temperature characteristics test platform is shown in Fig.4.

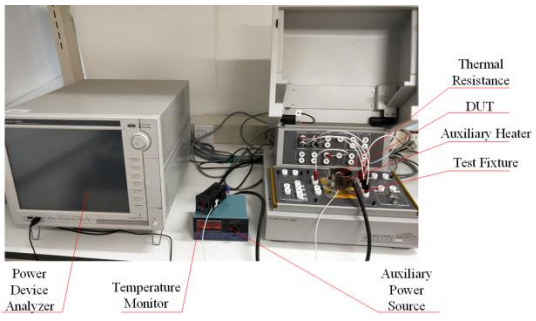

Fig. 4. *Temperature dependency of static parameters extracting test platform*

Since the gate bias voltage V_{GS} is relatively large after the SiC MOSFET turned on, the channel resistance R_{CH} will

have positive temperature characteristics as JFET region resistance R_{JFET} and drift region resistance R_D. Furthermore, due to the on-resistance R_{DS} can be regarded as the sum of R_{CH}, R_{JFET} and R_D, the on-resistance is also positively correlated with temperature [30].

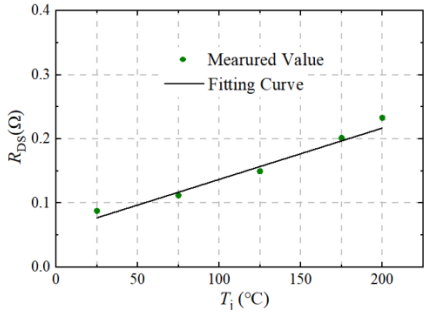

Fig. 5. *On-resistance of SiC MOSFET at different temperatures*

$$R_{DS} = a_{rds}T_j + b_{rds} = 0.0008T_j + 0.057 \quad (34)$$

As shown in Fig.5, the on-resistance R_{DS} of the SiC MOSFET changes by 0.145 Ω as the temperature rises from 25℃ to 200℃. R_{DS} can be approximated as a linear function of temperature. The fitting relationship can be expressed as (34), with the determination coefficient R^2 of the linear fitting being as 0.976.

When the SiC SBD working under the forward conducting state, the conduction voltage drop V_F can be regarded as the combination of Schottky contact forward voltage V_{FS} and the resistive voltage drop V_R, which can be expressed by the following equation:

$$V_F = V_{FS} + V_R = \frac{kT}{e}\ln\left(\frac{I_F}{I_S}\right) + R_F I_F \quad (35)$$

Where, I_F is the forward current of the SiC SBD, I_S is the saturation current, and R_F is the forward conduction resistance.

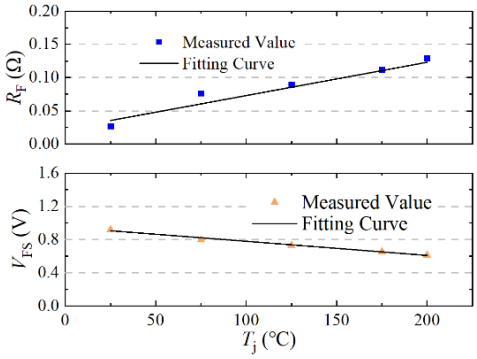

Fig. 6. *Forward onset characteristics of SiC SBD at different temperature*

Since I_S increases greatly with increasing temperature, the temperature coefficient of V_{FS} is negative. The measurement results are shown in Fig.6. The V_{FS} of the SiC SBD decreases approximately linearly with increasing temperature, while the forward conduction resistance R_F has positive temperature characteristics at 200 °C. V_{FS} is reduced by 0.3V compared with its value at room temperature while R_F is increased by 0.1Ω. The two temperature characteristic curves are fitted, and the relationship is shown in the following equations. The fitting coefficients for two linear functions are 0.985 and 0.955.

$$R_F = a_{rf}T_j + b_{rf} = 0.0005T_j + 0.023 \quad (36)$$

$$V_{FS} = a_{vfs}T_j + b_{vfs} = -0.0017T_j + 0.95 \quad (37)$$

3.2. Dynamic Parameter Extraction

Switching loss plays an important role in the total power loss of SiC MOSFET especially in high frequency applications. In order to extract the dynamic switching loss of SiC MOSFET and its temperature characteristics, this paper designed a double pulse test bench as shown in Fig.7.

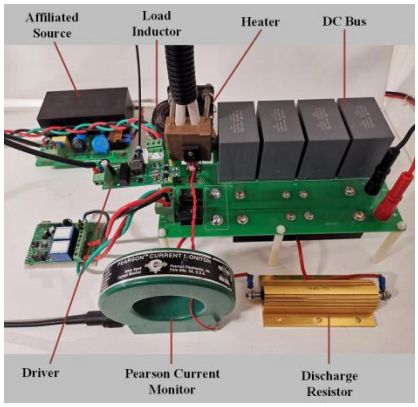

Fig. 7. *Double pulse test bench*

The test bench consists of a heater, power supply, DC capacitor bus, driver, load inductor and discharge resistor. Moreover, a Pearson current monitor with a ferrite bead is adopted for current measurement.

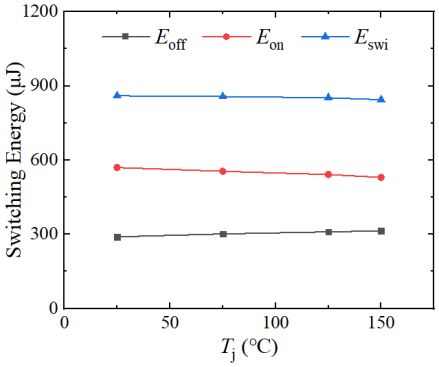

Fig. 8. *Switching energy at different temperatures*

The switching characteristics of SiC MOSFET were tested using the test bench at different temperatures under 500V/30A. According to IEC 60747-8 standard, turn-on switching energy E_{on}, turn-off switching energy E_{off} and total switching energy E_{swi} are tested and shown in Fig.8. For SiC MOSFETs, the threshold voltage decreases with increasing temperature. When the device turns on, a lower threshold voltage leads to faster turn-on transient, shorter turn-on time, and lower turn-on energy. During the turn-off period, a lower threshold voltage means the device will turn off later, thereby

increasing the turn-off transient time, and consequently increasing the turn-off transient energy loss by the way. Since the negative temperature characteristic of the turn-on energy and the positive temperature characteristic of the turn-off energy compensate each other, the temperature has little impact on total switching energy of SiC MOSFET.

4. Validation

4.1. Establishment of FEA Simulation Model

Based on the actual chip, layout and structure of a commercial 1200V/300A full SiC power module, a 1:1 finite element analysis 3D model was established using 3D design software as shown in Fig.9.

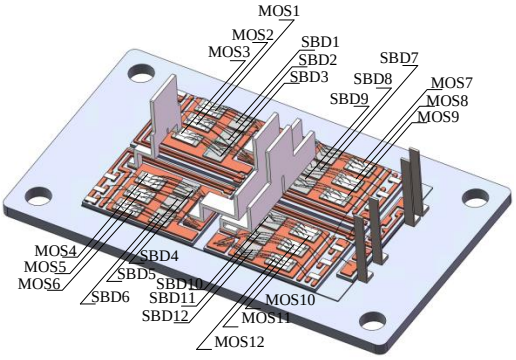

Fig. 9. *3D model for FEA simulation*

The module is a 6-chip parallel half-bridge module consisting of 12 SiC MOSFET chips and 12 SiC SBD chips. The chips are connected by aluminium bonding wires, and the chips are laid out on a DBC board of copper-alumina ceramic-copper three-layer structure. The lower layer of the DBC board is soldered on a large copper heat-dissipating substrate. 12 SiC MOSFETs and 12 SiC SBDs are sequentially numbered MOS1-MOS12 and SBD1-SBD12.

The simulation conditions are set as follows. (1) Since the demand of electrical insulation design, the single-side cooling module is filled with silica gel with a small thermal conductivity. So, the module is adiabatic except for the bottom surface; (2) The bottom surface is set up upon consideration of the water cooling of the bottom surface. The boundary conditions are constant at 60 ℃. (3) According to the technical manual of the MOSFET and SBD chip used in the actual module, the peak current I_m of each chip is set to 36A. Furthermore, mean temperature is extracted from the FEA results as the junction temperature of each chip.

4.2. Thermal Network Model Validation

This paper presents a simplified thermal network model which is based on the thermal circuit and mathematical optimization. Some comparisons are designed to validate the accuracy of the proposed thermal network model for SiC module under practical working conditions.

Due to the positive thermal characteristics of R_{DS} and R_F, conduction losses of SiC MOSFET and SiC SBD increase with increasing temperatures. This paper supposes that the total power losses are maximum for the setup of the chips when bipolar SPWM control is deployed at a temperature of 150 ℃, switching frequency of 50 kHz, and with I_m equal to 36 A. The maximum value is calculated as 107.99 W for MOSFET and 31.75 W for SBD. In order to obtain the traditional full thermal network, 4, 6, 8, 12 FEA simulations are done for 4 chip, 6 chip, 8 chip and 12 chip models. After finishing building the FTN, 6 groups of temperature data under different practical power loss setups (No.1,3,5,7,9,11) were extracted from the model, which were used for the calculation with STN. Furthermore, two groups of comparison of the two thermal networks were conducted under practical working conditions and consistent power working conditions. The practical power setup is shown in Table. I, while the results of the comparisons are shown in Fig.10.

Table 1 Power Loss at Practical Working Conditions

No.	1	2	3	4	5	6
I_m(A)	6	9	12	15	18	21
f_s(kHz)	5	7	10	15	20	25
P_{mos}(W)	2.43	5.36	9.74	16.29	24.47	34.28
P_{sbd}(W)	0.88	1.98	3.53	5.51	7.94	10.80
No.	7	8	9	10	11	
I_m(A)	24	27	30	33	36	
f_s(kHz)	30	35	40	45	50	
P_{mos}(W)	45.74	58.84	73.59	89.97	107.99	
P_{sbd}(W)	14.11	17.86	22.05	26.68	31.75	

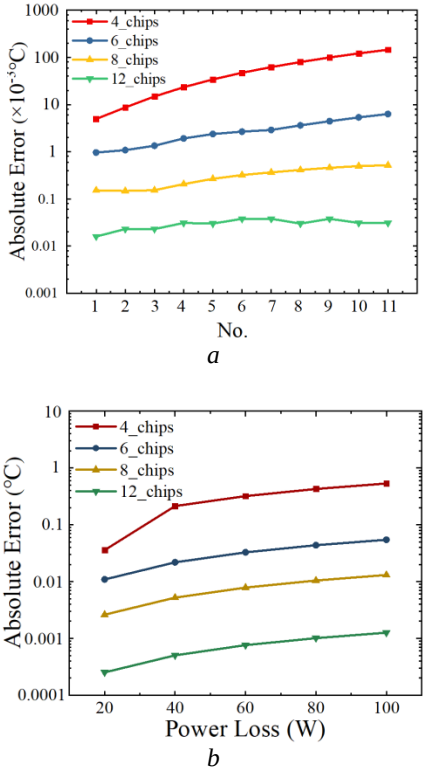

Fig. 10. *Comparison between FTN and STN at different working Condition*

(a) Practical working condition, ***(b)*** Consistent power working conditions

Whether the thermal network works under consistent power or under practical working conditions, the results of

the comparison between STN and FTN show the same conclusion. That is the absolute error increases with the increasing power loss and decreasing number of chips. Because of the unpractical power loss setup, the absolute error in consistent power working condition is larger. The maximum error in consistent power and practical working conditions are less than 0.6℃ and less than 0.2℃ respectively when there are only 4 chips. It is also found that the absolute error will go down to less than 0.002℃ and less than 0.00003℃ respectively if the network contains 12 chips. On the basis of the comparisons mentioned above, the accuracy of the STN used for SiC power module is satisfactory.

4.3. Thermal Network extraction

In this paper, an analytical junction temperature predicting model is proposed based on the thermal network model. In order to extract the thermal network used for temperature predicting, six finite element simulations of the 3D model of SiC module were carried out under six different working conditions the same as those used in thermal network validation. And junction temperatures of 24 chips are extracted. Based on the thermal network optimization model proposed above, the finite element simulation results are brought into the model, and the conjugate gradient method is used to iteratively optimize the calculation. The thermal network model for the minimum virtual temperature difference coefficient S of the module used in the simulation example is obtained. The thermal resistance values in the thermal network are shown in Fig.11.

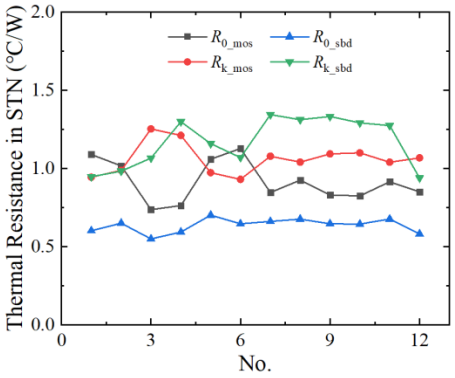

Fig. 11. *Results of the extraction of thermal resistances of SiC module*

Under different working conditions, the maximum difference of 24 virtual temperatures is 1.19 °C, the virtual temperature comprehensive difference coefficient S is less than 0.0043°C^2, and the average difference of the virtual temperatures of the two branches is 0.354 °C. The difference of the virtual temperature T_k between each branch is very small, and it can be approximated that all virtual temperature points have the same temperature. The analytical temperature predicting model based on the star thermal network can be used to predict and analyze the junction temperature.

4.4. Junction Temperature Predicting Model Validation

In order to verify the accuracy of the proposed junction temperature predicting model for electro-thermal coupling of SiC MOSFET module and study the influence of different factors on the temperature distribution of SiC MOSFET module, this paper uses the relative error e as shown in (38) to measure the difference between the finite element analysis and the calculated values of the model.

$$e = \frac{2\left|T_{\mathrm{jFEA}} - T_{\mathrm{jmod}}\right|}{T_{\mathrm{jFEA}} + T_{\mathrm{jmod}}} \tag{38}$$

Where, T_{jFEA} is the temperature calculated by finite element analysis, and T_{jmod} is the junction temperature predicted with the model.

The finite element calculation is performed on the SiC MOSFET module model under the unipolar and bipolar SPWM control. The temperature distribution diagram of the module is drawn as shown in Fig.12 according to the finite element calculation result under the 50 kHz switching frequency unipolar SPWM control. As shown in Fig.12, the SiC MOSFET and SBD chips in the module are the heat sources, and their temperatures are high. However, due to the difference in package structure design and inter-chip layout, there are some differences in the temperature of different chips. The SBD chip has a lower temperature than the MOSFET chip due to less heat generation.

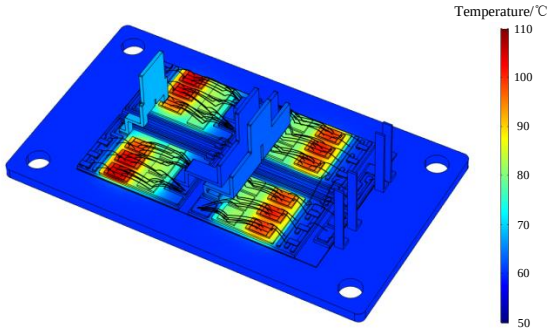

Fig. 12. *Temperature distribution of finite element calculation of SiC MOSFET module under unipolar SPWM control*

The switching frequency f_s was found to have a significant effect on the switching losses of all MOSFET chips. Consequently, the b value of SiC MOSFET chips will change as f_s changes. It is deduced from the previous analysis that f_s has a linear effect on the junction temperature of MOSFET and SBD chips. Changing the switching frequency from 10kHz to 40kHz, the distribution of predicted junction temperature by the proposed model was obtained. At the same time, the predicted and simulated results of MOS1 are compared and the relative error is calculated. The results are shown in Fig. 13.

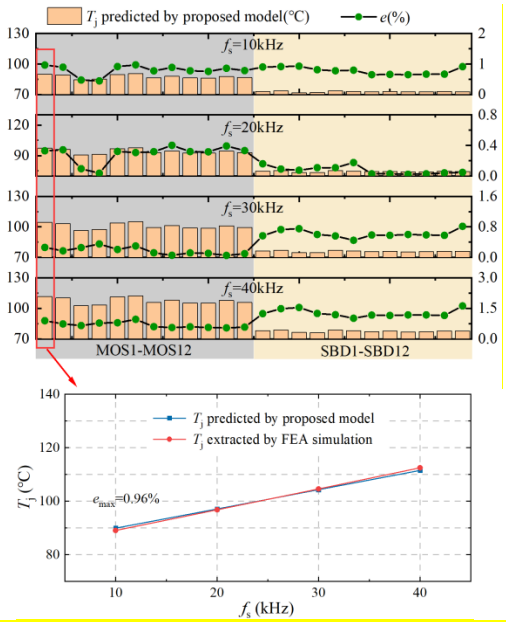

Fig. 13. *Predicted junction temperature distribution and the relative error under different switching frequency*

From the Fig.13, we can see that the finite element simulation and the proposed model predicting results show that the junction temperature of the chip varies linearly with the switching frequency f_s. This verifies the analysis of the analytical model. Compared with the results obtained from finite element simulation, the error of the temperature predicting model proposed in this paper is small. The maximum relative error of the junction temperature of MOS1 is only 0.96%. The accuracy of the model predicting results can be considered to be good.

The temperature coefficient a_{rds} of a chip's own on-resistance mainly has a direct effect on the temperature coefficient of the total heating power of the chip. And the heating power of other chips indirectly affects the temperature by heat transfer. It can be concluded from the above analysis that the chip temperature T_j is nonlinearly related to the chip temperature coefficient a_{rds}. The relationship between predicted T_{j_mos1} and a_{rds1} as well as the comparison between the predicted and simulated values obtained in a small a_{rds1} range are shown in Fig.14.

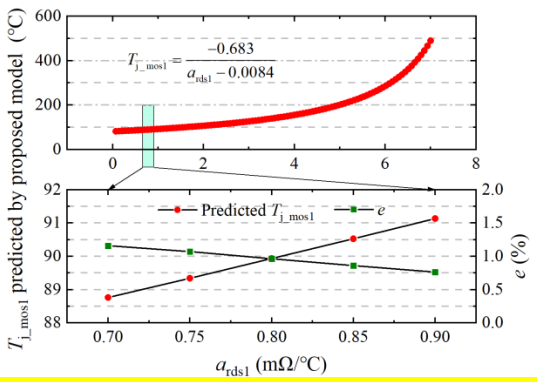

Fig. 14. *The relationship between predicted T_{j_mos1} and a_{rds1} as well as the comparison between the predicted and simulated values obtained in a practical a_{rds1} range*

As can be seen from Fig.14, when the a_{rds} range is large, the junction temperature T_j and a_{rds} exhibit a nonlinear relationship. The fitting is performed according to the analytical relationship obtained in the previous sections, and the determination coefficient R^2 is 1. However, in practical working conditions, the temperature coefficient dispersion of the on-resistance is not particularly large, usually between 0.7-0.9 mΩ/℃. After narrow the range of a_{rds}, we can see that the relationship between T_j and a_{rds} are approximately linear. Compared with the finite element simulation, the maximum relative error in the calculation made by the proposed model is 1.16% and the result can be rendered satisfactorily accurate.

5. Conclusion

Based on the temperature dependency of parameters of SiC MOSFET and SiC SBD, the power loss model of the chips in SiC module is obtained. The equivalent thermal network model based on virtual temperature is obtained by the conjugate gradient method. This equivalent model greatly simplifies the complexity of the network and facilitates the extraction of the thermal network and the calculation of the junction temperature. Based on this equivalent thermal network model and the power loss model, the analytical junction temperature predicting model of the the module is obtained. Using this model, the analytical relationship between the junction temperature of the chip and different influencing factors can be derived. Taking the results of finite element simulation calculation as a comparison, the relative errors of the analytical model's junction temperature predicting results proposed in this paper is very small, mostly less than 1.5%. Taking the switching frequency and the thermal characteristics of the on-resistance of the chip as an example, the validity of the analytical relationship derived from the analytical model is verified. The proposed junction temperature predicting model considering the internal electrothermal coupling can be used to estimate the temperature distribution of the internal chips of the SiC module. The model can further be used to analytically analyze the coupling relationship between different factors with the junction temperature.

6. Acknowledgment

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