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Comparison of TSEP Performances Operating at Homogeneous and Inhomogeneous Temperature Distribution in Multichip IGBT Power Modules

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***Abstract* — Temperature Sensitive Electrical Parameters (TSEPs) are used to determine the chip temperature of a single-chip IGBT power module by measuring one electrical device parameter. Commonly, most TSEPs have a linear relationship between the chip temperature and the electrical parameter. Like any sensor, preferred attributes of TSEPs include good accuracy, linearity, and sensitivity. For multichip Insulated Gate Bipolar Transistors (mIGBTs) modules, these can only be achieved when all chips have the same temperature. Equal chip temperatures among different semiconductor chips can be achieved when placing mIGBTs in environmental chambers to produce a homogeneous temperature distribution (HTD). In real applications, however, mIGBTs are power cycled and are exposed to inhomogeneous temperature distribution (ITD) where temperature differences exist between chips. Consequently, measuring one electric parameter only cannot represent each chip temperature which impacts the TSEP sensitivity, linearity, and accuracy. This paper compares the performance of ten TSEPs applied to a mIGBT module operating at HTD and ITD conditions in order to determine which TSEPs are most suitable for mIGBTs in real applications.**

***Index Terms*—Insulated gate bipolar transistor, multichip modules, global virtual junction temperature, temperature estimation, electrothermal effect.**

I. Introduction

Nowadays, Insulated Gate Bipolar Transistor (IGBT) power modules are manufactured by means of multichip package technique to complement the power density limitation of the IGBT chip material and achieve a higher power capability. The high power density of these multichip IGBT (mIGBT) modules causes thermal stress. IGBT power modules have a multi-layered structure incorporating different materials. The mismatch of materials' coefficient of thermal expansion (CTE) introduces mechanical stress between adjacent layers [1, 2] which consequently leads to thermos-mechanical failures. It is reported that about 21% of power electronic system failures are caused by semiconductor power devices [3]. Therefore, knowledge of accurate junction temperature T_j is essential to reliability improvement and design optimization of power devices.

While the virtue and performance of mIGBTs are often evaluated at specified temperatures at given locations (e.g. ambient, case, and junction), the junction temperature becomes widely used when considering maximum temperature ratings and long-term reliability of IGBT modules. It is an important operating condition representing the temperature within the junction region, typically a thin power dissipating layer within the semiconductor chip. Although in actual practice, temperature differences occur within and between chips, it appears to be a reasonable compromise to give junction temperature a uniform value, called global virtual junction temperature (T_{vj}). T_{vj} is a pivotal parameter for thermal network analysis [4] and to derive the thermal impedance between junction and case [5, 6] which is crucial for thermal performance characterization and thus reliability prediction.

Despite numerous junction temperature measurement techniques, the electrical method based on Temperature Sensitive Electric Parameters (TSEPs) is found in prevalent use that has been demonstrated by many researchers. Some typical advantages of using TSEPs include non-intrusive measurement, fast dynamic response, and the monotonic and linear relationships with T_{vj}. Table I provides an overview of some exemplar TSEPs applied to single-chip and multichip (or both) IGBT modules.

TABLE I

SUMMARY OF SELECTED TSEPS

TSEPs	Single-chip /Multichip	Sensitivity(/°C)	Reference
$V_{CE(on\text{-}load)}$	Both	1mV - 4mV ↑	[7-10]
$V_{CE(on\text{-}sense)}$	Both	4mV - 10mV ↓	[7-10]
$R_{g(int)}$	Both	0.9mΩ - 2.8mΩ ↑	[11-14]
$\Delta V_{CE(\Delta VGE)}$	Single-chip	2.5mV ↑	[10]
$I_{C(short)}$	Single-chip	0.345A ↓	[15]
$V_{GE(th)}$	Single-chip	2mV - 10mV ↓	[4, 16-18]
$\int I_{GE}$	Single-chip	0.3nC ↑	[19]
$t_{d(on)}$	Single-chip	2ns ↑	[20]
$t_{d(off)}$	Single-chip	1.01.ns ↑	[21]
$V_{GE(Miller)}$	Single-chip	4.7mV ↓	[21]
dV_{CE}/dt	Single-chip	6V/μs ↓	[22]
$I_{C(tail)}$	Single-chip	51mA ↑	[21]
$\int V_{GE}$	multichip	70mV ↓	[23]
t_{Miller}	multichip	0.8ns - 3.4ns ↑	[21, 24]
g_m	multichip	1.54A/V ↓	[25]
V_{cE}	multichip	68mV ↑	[26]
$V_{pre(th)}$	multichip	2.2 mV ↓	[27]

↑ TSEP has a positive temperature coefficient.
↓ TSEP has a negative temperature coefficient.

As shown in Table I, TSEPs have been successfully used for single-chip IGBT power devices. That is because there is a clear relation between the measured electric parameter and T_j. The same relation between the electric parameter and chip temperatures in mIGBTs applies when each chip has the same T_j. In this case, T_{vj} is equal to T_j. This scenario can be performed in the laboratory by using a heat plate or an environmental chamber so that all chips can be evenly heated externally and reach the same junction temperature.

Typically, TSEPs are applied in two steps. The first step is calibration where mIGBT modules are heated in a controlled temperature environment and the electric parameter is measured for each temperature change. This produces a reference baseline between the electric parameter and T_{vj}. Once the mIGBT is operating in the field, it measures the electric parameter and calculates T_{vj} from the recorded baseline.

Although the above procedure seems uncomplicated as being widely demonstrated using single-chip IGBTs, it faces a fundamental problem for mIGBTs. When producing the baseline, homogenous temperature distribution (HTD) among all chips is performed for mIGBT modules. However, once a mIGBT module is operating in the field, it is power cycled, producing switching losses and conduction losses that result in inhomogeneous temperature distribution (ITD) between chips. That is because the junction temperature of the individual chips varies due to differences in heat dissipation and differences in the thermal impedance caused by tolerances in chip manufacturing and packaging layouts. For instance, a 5°C to 15 °C dissimilarity was observed between the hottest chip and the coldest chip in a power cycled mIGBT module [13, 28]. Consequently, the baseline does not match once the mIGBT is operating in the field which raises concerns about the appropriateness of TSEPs for mIGBTs. To the authors' knowledge, no study has been published that compares the performance of TSEPs at ITD conditions. This paper assesses the accuracy, linearity, and sensitivity of TSEPs at HTD and ITD by experiment and discusses the limitations for each TSEP.

The paper is structured as follows. Section II describes online operation tests in an mIGBT module with the thermal performance recorded via an infrared camera. The Spatial Distribution of Temperature (SDoT) is evaluated at power-module level. Section III introduces selected TSEPs and their temperature dependency. Section IV describes the experimental setup for both HTD and ITD conditions. Experimental results at both HTD and ITD conditions are compared in Section V. Section VI concludes the findings drawn from this study.

II. Temperature Distribution in Multichip Module

Despite the paralleled configuration of the multichip power module, ITD exists between chips due to variations in chips, layouts, and structures. Tests to evaluate the thermal distribution have been carried out for an open mIGBT module (FF600R17ME) from Infineon to investigate its temperature distribution for one power pulse. FF600R17ME4 is a half-bridge module with one high-side switch and one low-side switch. Each switch consists of three IGBT chips in a parallel connection. For the investigation, a three-chip module was deliberately chosen to differentiate three temperature statuses: Hottest-Medium-Coolest.

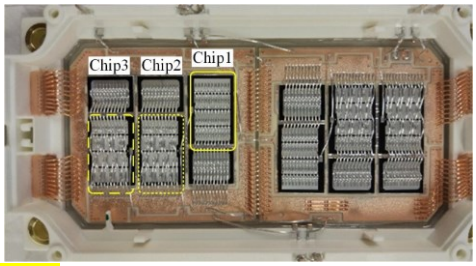

Fig. 1. The layout of the FF600R17ME4 IGBT Module.

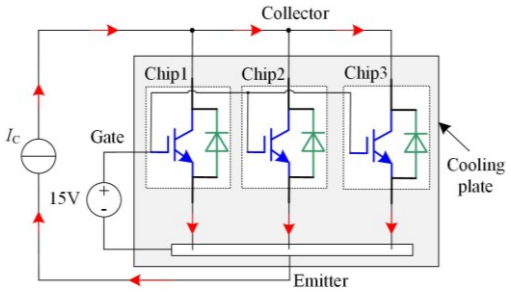

Fig. 2. Schematic of the experimental setup.

Fig. 1 gives an aerial view of the open module, with the switch on the left used for temperature measurement. The IGBT chips are highlighted in boxes and annotated as Chip1, Chip2, and Chip3, respectively. The schematic of the experimental setup is shown in Fig. 2. The module is mounted on a water-cooling plate which is controlled by a chiller (µC2SE for process chiller). The temperature of the cooling plate is set at 20°C. The gate of the IGBT module is biased at +15 V and the load current is controlled using a TopCon DC power supply. The SDoT of the mIGBT is captured by the infrared camera FLIR 6700. Fig. 3 shows the configuration of the test rig.

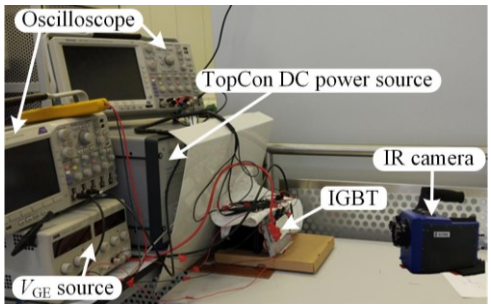

Fig. 3. Setup for the power cycling test.

Fig. 4a depicts the injected current pulse and the corresponding transient temperature response. At t_0, the current starts to ramp up and the temperature increases with the current as shown in Fig. 4a. At t_1, the current reaches the set value I_C and is hold until t_2 where the current is switched off. The operating conditions of the IGBT are varied by regulating the pulse length (t_2-t_1) and the current level I_C. The temperature distribution is evaluated by analyzing the IGBT chip's junction temperatures at t_2.

In this test, 300A and 420A are selected for I_C, which represent 50% and 70% of the rated current of the power module, respectively. The pulse length ($t_{pulse} = t_2$-t_1) varies from 1s to 15s.

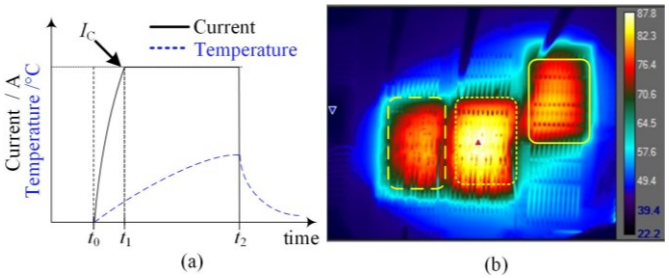

Fig. 4. Temperature distribution. (a) Temperature alteration against current pulse injection. (b) Temperature distribution of the IGBT switch at t_2 when I_C = 300 A and t_{pulse} = 12s.

The average temperature within each chip in Fig. 4b is the junction temperature of the IGBT chip, denoted as $T_{j\text{-}Chip\,i}$, where i in the subscript is the chip number 1, 2, or 3.

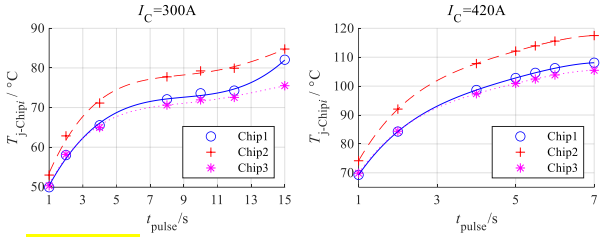

Fig. 5. The junction temperature of IGBT chips versus pulse length t_{pulse} at I_C = 300 A and I_C = 420 A.

R3.2 Fig. 5 shows the real-time junction temperature measurements as a function of time, t_{pulse}, in response to a constant heating current pulse I_C. It can be noticed that there is inhomogeneous temperature distribution among the three chips. While the junction temperature T_j of each IGBT chip increases with pulse width, Chip2 is the hottest followed by Chip1 and Chip3. There is constrained heat spreading as heat conducts from chip through the package to ambient due to the physical position of Chip2 in between other chips. Fig. 6 shows the maximum junction temperature differences between chips, namely the difference between Chip2 and Chip3. At I_C = 300 A, the variance ($T_{j\text{-}Chip2}$- $T_{j\text{-}Chip3}$) is 9 °C at t_{pulse} = 15 s. The variance ($T_{j\text{-}Chip2}$- $T_{j\text{-}Chip3}$) is 12 °C at t_{pulse} = 7 s for I_C = 420 A. Note that tests at I_C = 420 A were stopped at 7 s to maintain the IGBT within the safe temperature range.

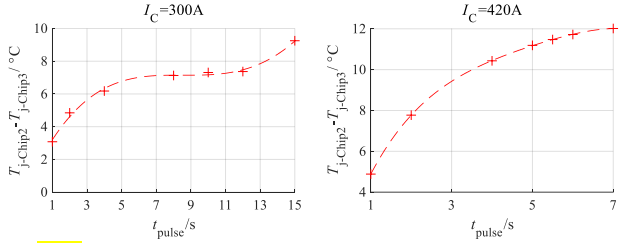

Fig. 6. The temperature variance between Chip2 and Chip3.

It can be concluded from Fig. 5 and Fig. 6 that significant ITD occurs between different chips when the mIGBT is power cycled driven by current loads and the temperature variance increases with pulse width. The next section illustrates common TSEPs and their temperature dependency.

III. Selected TSEPs for T_{VJ} Prediction

R1.1 This section provides an overview of the most popular TSEPs. Fig. 7 exemplifies the typical switching waveforms of an IGBT module with eight selected electrical parameters annotated.

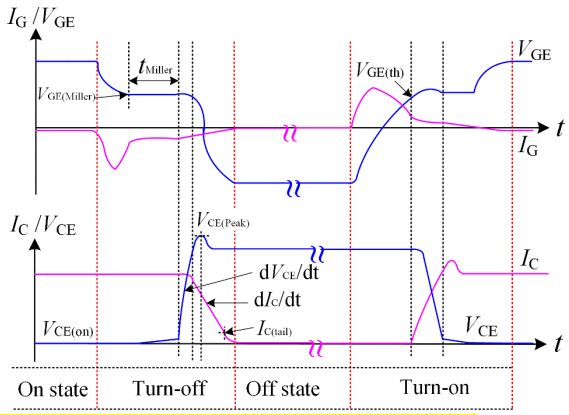

Fig. 7. Illustration of typical switching waveforms of an IGBT.

Among them, $V_{CE(on)}$ is the most prevailing approach due to its high reliability and long measurement window during the IGBT on-state and has been described in [29]. The collector current I_C can be either a low sense current $I_{C(sense)}$, where the corresponding on-state voltage $V_{CE(on\text{-}sense)}$ is dominated by the forward voltage drop in the base region of the pnp-transistor thus manifesting a negative temperature coefficient, or a load current $I_{C(load)}$, where the on-state voltage $V_{CE(on\text{-}load)}$ is mainly influenced by the on-state impedance of the IGBT exhibiting a positive temperature coefficient.

During the switching transient, the gate-collector capacitor C_{GC} and gate-emitter capacitor C_{GE} are charged/discharged and the gate-emitter voltage V_{GE} and gate-emitter current I_{GE} undergo the Miller plateau during the transients as shown in Fig. 7 [21]. The duration of the plateau t_{Miller} is also temperature-dependent [21, 24], but depends also on V_{CE} and I_C [24]. Generally, $V_{GE(Miller)}$ and t_{Miller} at turn-off have good temperature sensitivity and linearity.

dV_{CE}/dt and dI_C/dt at turn-off are the collector-emitter voltage slope and current slope, respectively. dV_{CE}/dt is described in [22]. dV_{CE}/dt does not only depend on temperature, but also V_{CE} and I_C levels. The temperature dependency of dI_C/dt has been derived and verified in [30, 31].

R2.1 Another current related TSEP is $I_{C(tail)}$ [29]. During the turn-off transient, there are two stages of the declining I_C. In the first stage, the current decays fast followed by a slower decay in the second stage which is often called tail current. At the start of the tail current the minority carrier lifetime is highly temperature dependent thus $I_{C(tail)}$ can be classified as a TSEP.

$V_{CE(peak)}$ has also been employed to estimate junction temperature [32, 33] which shows good linearity with temperature. Another TSEP is reported in [16] called threshold voltage $V_{GE(th)}$ which is the gate voltage at which the IGBT turns on and collector current begins to flow. Trans-conductance g_m is introduced in [25]. It is assumed that the instantaneous change of I_C is proportional to V_{GE} at a fixed V_{CE}. Since the temperature compensated resistor will influence collector current I_C distribution, trans-conductance g_m will also vary with temperature.

R1.2 The relationship between T_j and the electrical parameters applies so long the TSEP is connected to a single-chip power

module or a multichip module operating at HTD. That is because any TSEP measures only one electrical parameter that is linked to only one temperature. However, HTD can only be produced in the laboratory by externally heating the power module in a controlled manner without power switching the device. HTD does not represent a real working environment in field applications when mIGBTs are switched and heat due to switching and conduction losses is produced which results in ITD. Consequently, there is no clear relation between the single electrical parameter and the individual junction temperatures of each chip.

IV. Experimental Setup

A special heat plate has been designed to establish the uneven temperature distribution conditions, shown in Fig. 8a. The heat plate consists of two temperature-controlled plates, a water-cooling cold plate and an electronic hot plate. The cold plate is connected to a temperature-controlled chiller (μC^{2}SE) with coolant temperature set to 15°C hereinafter. The hot plate temperature is regulated by the thermostat, which provides a span of temperature between 45°C and 200°C. A thermal insulation layer (Calcium-Magnesium Silicate Thermal Insulation Sheet) is inserted between both plates to suppress the thermal conduction between them. With this heat plate, the temperature of Chip1 and Chip2 can be adjusted, so that it is different from Chip3. A trapezoidal slot is grooved in the base plate of the IGBT, as shown in Fig. 8b. The slot is between Chip2 and Chip3 which aids to minimize the thermal conduction across the baseplate.

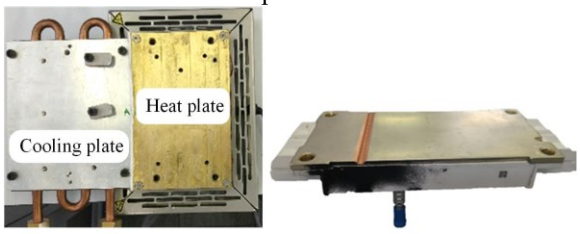

Fig. 8. (a) Hot plate and cold plate for T_{vj} control. (b) The groove in the baseplate of the IGBT.

The FLIR 6700 infrared camera is set to monitor the temperature distribution of the mIGBT, which, like tests before, is coated with matt black paint to ensure that the emissivity of the chip surface approaches 0.95.

A. Static TSEP rig

$V_{CE(on\text{-}load)}$ and $V_{CE(on\text{-}sense)}$ are well known static TSEPs and are applied during the on-state of the device. The test rig for their measurement is built according to Fig. 2. $V_{CE(on\text{-}load)}$ is measured at 300 A load current, while $V_{CE(on\text{-}sense)}$ is captured with a sense current of 100 mA.

B. Dynamic TSEP rig

Dynamic TSEPs are extracted from switching transient waveforms, which can be captured using oscilloscopes with dedicated probes in a double pulse circuit as illustrated in Fig. 9a. The switching sequence is illustrated in Fig. 9b. Phase t_0 - t_1 is to allow the current to build up. At the turn-off transient of the first pulse t_1 and the turn-on transient of the second pulse t_2, the collector-emitter voltage and the collector current remain constant $V_{CE1} = V_{CE2}$ and $I_{C1} = I_{C2}$. This ensures that TSEPs are tested in the same operational condition. Therefore, electrical parameters during the turn-off and turn-on transient are comparable.

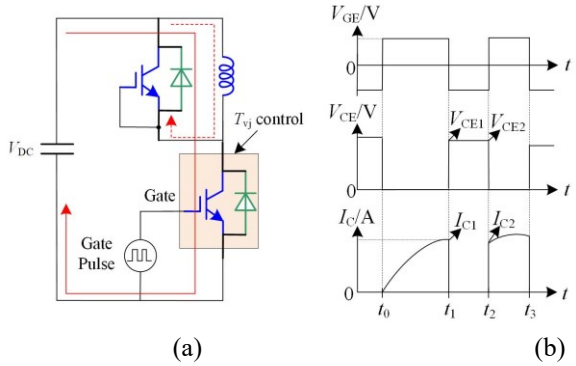

Fig. 9. (a) Double pulse test circuitry. (b) Double pulse switching sequence.

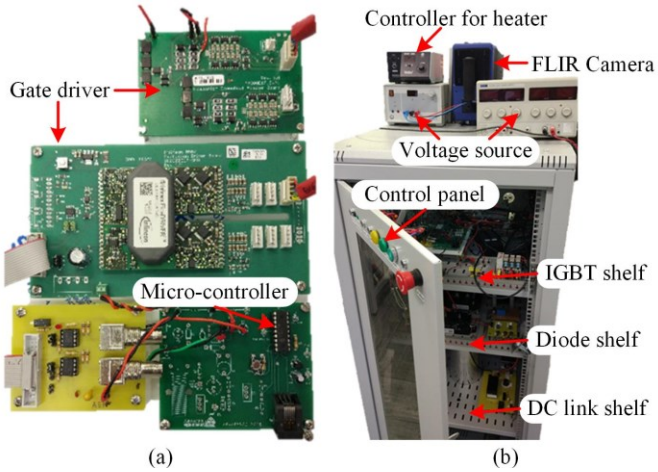

Fig. 10. (a) Gate driver. (b) Double pulse test platform.

The corresponding test rig is shown in Fig. 10. The gate driver includes two commercial driver boards and a micro-controller PIC16F819 for gate pulse regulation. V_{CE}, I_C, V_{GE}, and I_G are measured using the oscilloscope Tektronix MSO 4034 and DPO 3014. R2.2

The mIGBT is a 600A/1700V device and the operating voltage was 225V and the operating current was 150A. The reason for limiting voltage and current was because tests had to be conducted on an open module without insulation (no gel). Thus, the test conditions had to be derated. It should be added that sensitivity and linearity do change slightly with operating voltage and current. That is because semiconductor device parameters of TSEPs are influenced by the applied voltage, current, and turn-on and turn-off speed. [34, 35]. For comparison reason, all operational parameters have been kept constant.

V. Results and Discussion

A. Tests under HTD conditions

It has been reported that TSEPs can be applied to HDT conditions [4]. That is because at HTD T_j of each chip is equal, resulting in T_{vj}=T_j. Consequently, the temperature for each chip

is known. However, knowledge of the temperature alone is not sufficient. Like with any sensor, sensitivity and linearity are also important. Thus, this section compares the sensitivity and linearity of TSEPs applied to mIGBT at HTD conditions and establish the benchmark for later uses to be compared with those at ITD conditions.

The power module was mounted on the top of the hot plate only (the water-cooling plate was not used for HTD) in the calibration step and the external hot plate temperature is adjusted by the thermostat. A sufficient period of time was given prior to the TSEP measurement so that a quasi-thermal equilibrium for heat condition was reached.

The maximum temperature divergence between any chips was no more than 0.5°C. This appears to be a reasonable assumption that HTD is reached. The hot plate was set to five different temperatures and the corresponding global virtual junction temperature T_{vj} of the mIGBT switch was derived with equation (1) [4-6].

R3.4

$$T_{vj} = \left| \frac{\sum_{i=1}^{3} T_{j,Chipi} S_i}{\sum_{i=1}^{3} S_i} \right| = \left| \frac{T_{vj,1}S_1 + T_{vj,2}S_2 + T_{vj,3}S_3}{S_1 + S_2 + S_3} \right| \quad (1)$$

where i is the chip number and S_i is the surface area of the i-th chip. The current was measured using a Rogowski coil wrapped around bond wires. The coil covers part of the chip during temperature measurements. The areas that were accessible for temperature measurement S_i are shown in Fig. 4 and Fig. 15 (note both figures show the current sensor removed) and these areas are used in (1).

In these five tests, the global virtual temperature of the mIGBT switch were $T_{vj,1}$=22.1°C, $T_{vj,2}$=46.2°C, $T_{vj,3}$=62.0°C, $T_{vj,4}$=75.8°C, and $T_{vj,5}$=89.8°C. Table II shows the temperature condition of each chip at HTD conditions.

R3.5

TABLE II TEMPERATURE CONDITION FOR HTD TESTS

Test No.	$T_{j\text{-}Chip1}$/°C	$T_{j\text{-}Chip2}$/°C	$T_{j\text{-}Chip3}$/°C	T_{vj}/°C	Δ_{Max}/°C
1	22.0	22.1	22.1	22.1	0.1
3	61.9	62.2	62.0	62.0	0.3
4	75.6	76.0	75.8	75.8	0.4
5	89.7	90.0	89.6	89.8	0.4

Fig. 11 shows the turn-off transient of V_{GE} with its corresponding Miller plateau level and the Miller plateau width given in an enlarged view. It can be observed that the Miller plateau voltage is decreasing with the rising temperature T_{vj}, while the Miller plateau width increases with temperature T_{vj}.

Fig. 12 shows the turn-on transient of V_{GE}. The zoomed view shows that $V_{GE(th)}$ decreases with rising T_{vj}. Fig. 13 and Fig. 14 are the turn-off transient of I_C and V_{CE}, respectively. These two figures also enable the derivation of the switching characteristics of dV_{CE}/dt, dI_C/dt, $V_{CE(peak)}$, and $I_{C(tail)}$.

R2.1

The voltage slope dV_{CE}/dt is derived from the V_{CE} switching edge between 90% and 10% of the DC-bus voltage. The current slope dI_C/dt is measured between 80% and 20% of I_C. $I_{C(tail)}$ is measured at a unified time stamp t=301.68 µs at which the tail current starts at for the test condition with junction temperature at 22°C. Additionally, with the measurement of V_{GE} and I_C, g_m can be deduced.

The sensitivity and linearity of the selected TSEPs are calculated and compared in Table III, with both attributes derived based on equations (2) and (3) respectively.

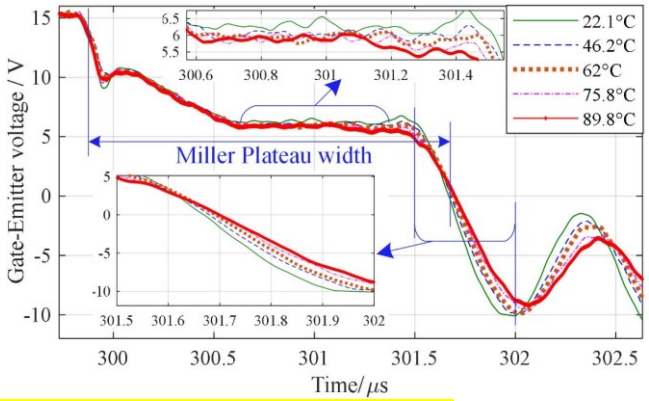

Fig. 11. V_{GE} during turn-off transient at HTD condition.

R2.3

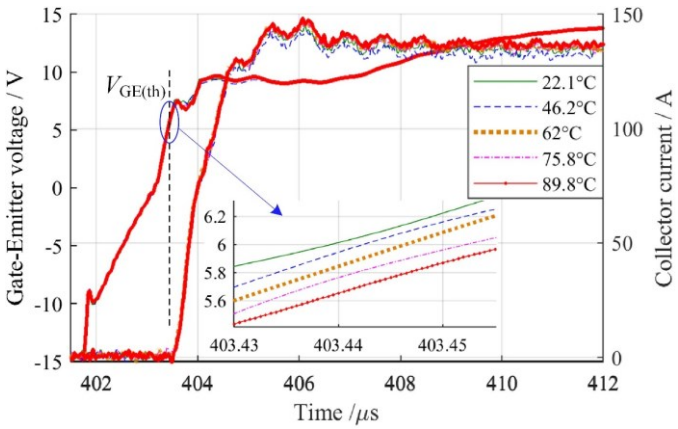

Fig. 12. V_{GE} during turn-on transient at HTD condition.

R2.3

$$sensitivity = \left| \frac{TSEP_{T_{vj,5}} - TSEP_{T_{vj,1}}}{T_{vj,5} - T_{vj,1}} \right| \quad (2)$$

where $TSEP_{Tvj,5}$ and $TSEP_{Tvj,1}$ are the TSEPs measured at $T_{vj,5}$ and $T_{vj,1}$, respectively.

$$linearity = \frac{\sum_{i=1}^{n} (TSEP_{f(i)} - TSEP_{m(avg)})^2}{\sum_{i=1}^{n} (TSEP_{m(i)} - TSEP_{m(avg)})^2} \quad (3)$$

where $TSEP_{m(i)}$ is the observed measurements and $TSEP_{f(i)}$ is the linear curve fitted values at the i-th measurement (i is 1, 2, 3, 4, 5). $TSEP_{m(avg)}$ is the average of all observed measurements and n is the number of total measurements at the reference temperature.

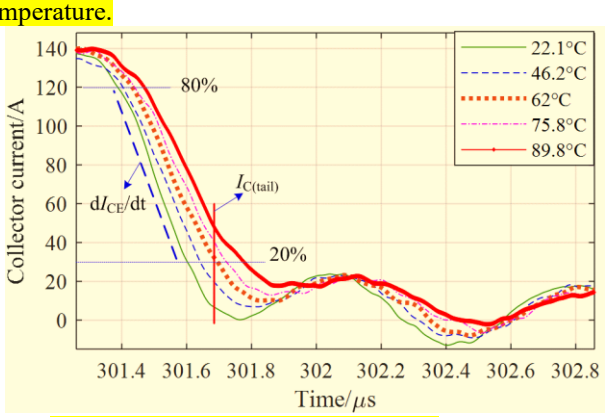

Fig. 13. I_C during turn-off transient at HTD condition.

R2.1

R2.3

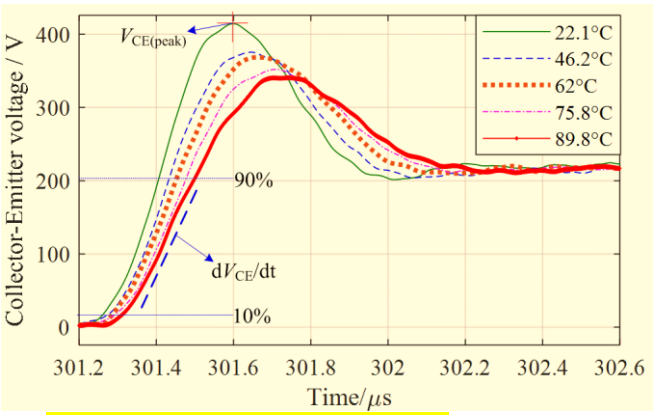

Fig. 14. V_{CE} during turn-off transient at HTD condition.

Take $I_{C(tail)}$ as an example. The measured current at $T_{vj,1}$ to $T_{vj,5}$ are $TSEP_{m(1)}$=4.5122A, $TSEP_{m(2)}$=16.7458A, $TSEP_{m(3)}$=27.3648A, $TSEP_{m(4)}$=33.3339A, $TSEP_{m(5)}$= 43.3155A. The average value of the five TSEPs is $TSEP_{m(avg)}$=25.0544A. The curve fit equation based on the least squares regression is $I_{c(tail)}$=0.5688T_{vj}-8.6071. The corresponding fit values are $TSEP_{f(1)}$ = 3.96338A, $TSEP_{f(2)}$= 17.67146A, $TSEP_{f(3)}$ = 26.6585A, $TSEP_{f(4)}$ = 34.50794A and $TSEP_{f(5)}$= 42.47114A. With (3), it can be derived that the linearity for $I_{C(tail)}$ is 0.9958. The sensitivity of $I_{C(tail)}$ can be calculated from (2) and is: |(43.3155A – 4.5122A)/(89.8°C – 22.1°C)|=0.573 A/°C. Table III summarizes sensitivity and linearity for all ten TSEPs.

TABLE III SENSITIVITY OF TSEPS

	TSEPs	Sensitivity(/°C)	Linearity
On State	$V_{CE(on-load)}$	2.75 mV ↑	0.9921
	$V_{CE(on-sense)}$	2.069 mV ↓	0.9948
Turn on	$V_{GE(th)}$	5.7 mV ↓	0.9894
Turn off	t_{Miller}	0.9 ns ↓	0.9411
	$V_{GE(Miller)}$	5.6 mV ↓	0.9393
	dV_{CE}/dt	10.06 V/μs ↓	0.9838
	dI_C/dt	2.007 A/μs ↓	0.8892
	$V_{CE(peak)}$	1.02V ↓	0.9645
	g_m	0.9358 S ↓	0.9861
	$I_{C(tail)}$	0.573 A ↑	0.9958

↑ Positive temperature coefficient.
↓ Negative temperature coefficient.

Table III confirms good linearities can be found for all TSEPs except dI_C/dt. The sensitivity of $V_{CE(on-load)}$ is slightly better than $V_{CE(on-sense)}$. The advantage of the two static TSEPs is that they require voltage sensors with low bandwidth. Dynamic TSEPs also demonstrate good sensitivities but do require costly sensors of high bandwidth and high sampling rate. Above all, the majority of TSEPs show good sensitivity and linearity at HTD conditions.

B. Tests at ITD conditions

For ITD tests, the mIGBT power module was mounted on the previously described heating-cooling combination plate shown in Fig. 8a. In this particular arrangement, Chip1 and Chip2 are over the hot plate while Chip3 is over the cooling plate. The chiller and electronic heater are individually controlled to establish different temperature gradients among three chips. Three tests were carried out, referred to as Test 1, Test 2, and Test 3. The chiller temperature was maintained at 15°C for all three tests, while the hot plate temperature varied from 48°C, 70°C to 90°C, respectively. These temperature conditions are specially chosen to emulate a range of ITD conditions with typical chip temperature differences that are likely to occur in practice as described in Section II.

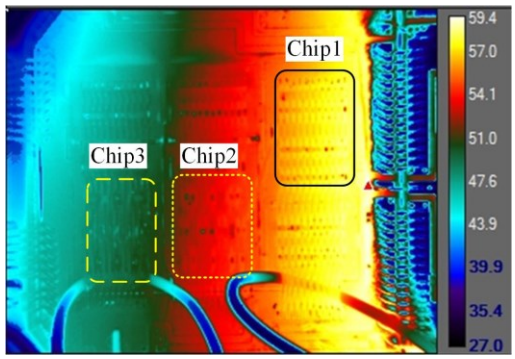

Fig. 15. Thermography of the mIGBTs module under test with the chiller set at 15°C and hot plate set at 90°C.

Fig. 15 is an exemplar view of the surface temperature map in the mIGBT module taken by the infrared thermographic camera. There is a distinct temperature variation between all three chips, with Chip1 being the hottest while Chip3 being the coldest.

While T_j of each IGBT chip is measured with the help of the thermal camera, the global virtual temperature T_{vj} of the mIGBT switch is derived with equation (1). The boxes in Fig. 15 highlights the surface area used to estimate T_j of each IGBT chip in the mIGBT module.

The corresponding temperature conditions are shown in Table IV. Similar to HTD, the temperatures have been recorded after a sufficient period so that each IGBT chip reached its quasi-thermal equilibrium. Δ_{Max} in Table IV represents the maximum temperature variance among the three chips. For instance, Δ_{Max} of Test 1 equals $T_{j\text{-}Chip,1}$ - $T_{j\text{-}Chip3}$.

Although the hot plate was adjusted from 48°C to 70°C and 90°C for Test 2 and Test 3, temperatures at Chip1 and Chip2 are much lower once the quasi-thermal equilibrium is reached. This is because thermal conduction still takes place through the thermal conduction paths of the DCB substrate and the residue connection of the base plate. A groove was cut into the base plate (Fig. 8b) to minimize thermal coupling. A residual connection was left to prevent the DCB and the power module from damages. This small residue of base plate material attached to the DCB still acts as a thermal path in addition to DCB itself all in opposition to the intended temperature disparity and allowing heat to conduct from Chip1 and Chip2 to the cold plate. However, the experimental setup achieves a reasonable reproduction of ITD conditions. For example, in Test 3, a maximum T_j difference of 8.7°C between all three chips was produced which is 16 times bigger compared to that at HTD conditions which had less than 0.5°C across all chips.

TABLE IV TEMPERATURE CONDITION FOR THREE TESTS

Test No.	$T_{j\text{-}Chip1}$/°C	$T_{j\text{-}Chip2}$/°C	$T_{j\text{-}Chip3}$/°C	T_{vj}/°C	Δ_{Max}/°C
Test 1	34.6	33.0	30.8	32.5	3.8
Test 2	45.7	44.0	40.4	43.5	5.3
Test 3	56.9	53.0	48.2	52.4	8.7

Table IV shows that the maximum temperature variance is always between Chip1 and Chip3 in all three tests. Table IV also presents T_{vj} based on equation (1) which are 32.5°C, 43.5°C, and 52.4°C for Test 1, Test 2, and Test 3, respectively.

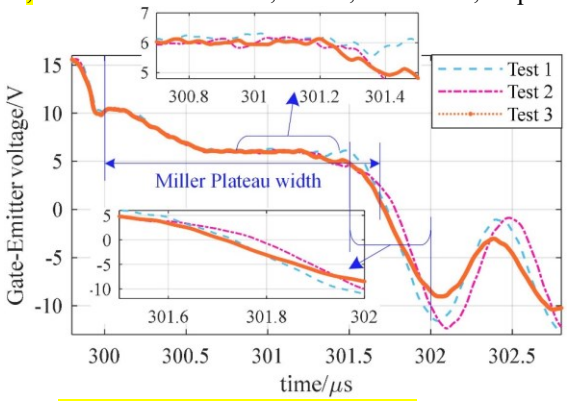

Fig. 16. V_{GE} during turn-off transient at ITD condition.

Double pulse tests were conducted to measure TSEPs under all three conditions. Fig. 16 and Fig. 17 show the switching transient of V_{GE} for turn-off and turn-on, respectively. As shown in Fig. 16, the Miller plateau voltage $V_{GE(Miller)}$ and the Miller plateau width t_{Miller} do not show a clear dependence on the temperature. The same conclusion is observed for $V_{GE(th)}$ during the turn-on transient. As all three TSEPs have no clear relationship with temperature changes under ITD, it is concluded that $V_{GE(Miller)}$, t_{Miller}, and $V_{GE(th)}$ are not suitable for T_{vj} estimation for mIGBTs in this experiment.

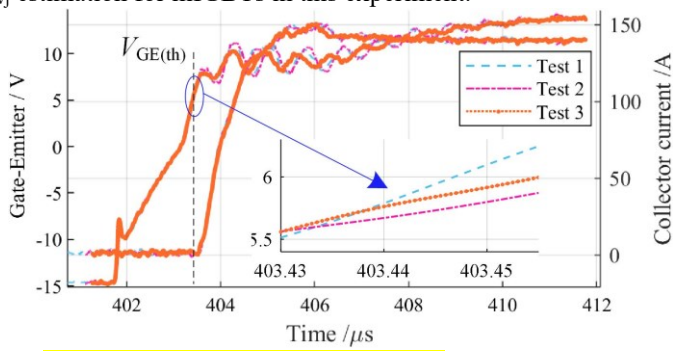

Fig. 17. V_{GE} during turn-on transient at ITD condition.

Fig. 18 and Fig. 19 are the turn-off transients for V_{CE} and I_C at ITD conditions, with dV_{CE}/dt, $V_{CE(peak)}$, g_m, and $I_{C(tail)}$ parameters extracted from these waveforms.

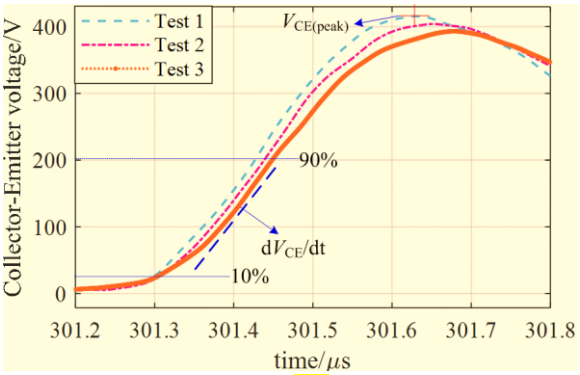

Fig. 18. V_{CE} during turn-off transient at ITD condition.

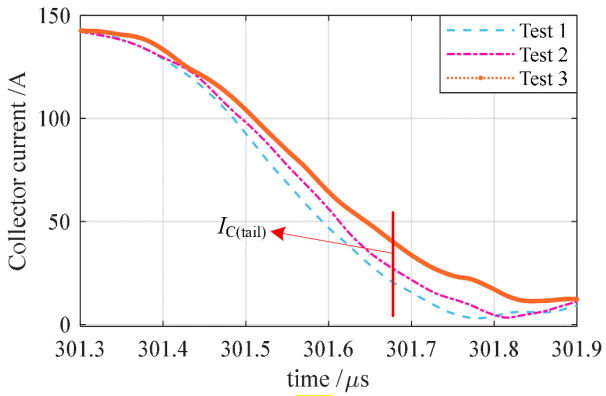

Fig. 19. I_C during turn-off transient at ITD condition.

Of ten TSEPs investigated at HTD, four TSEPs: $V_{GE(Miller)}$, $V_{GE(th)}$, t_{Miller}, and dI_C/dt don't show any linear relationship with the temperature at ITD conditions. The other four dynamic TSEPs, dV_{CE}/dt, $V_{CE(peak)}$, $I_{C(tail)}$, and g_m, and the two static TSEPs, $V_{CE(on\text{-}load)}$ and $V_{CE(on\text{-}sense)}$, are therefore further evaluated in terms of sensitivity and linearity. The results are plotted in Fig. 20. The black line and the blue dotted line represent linearized TSEPs under ITD and HTD conditions, respectively. Three red error bars indicate the temperature spread of the three chips in the mIGBT switch. Fig. 20 shows that TSEP $V_{CE(on\text{-}sense)}$ has a good overlap between HTD and ITD conditions. All other TSEPs show that their parameter diverts from each other with increasing temperature except $V_{CE(peak)}$, which narrows with increasing temperature. $I_{C(tail)}$ shows the biggest diversion between HTD and ITD. R3.6

Table V compares the accuracies for each TSEP at each test. It shows the temperature difference between the highest (T_{max}), middle (T_{mid}), and coolest (T_{min}) chip temperature from Table IV and the virtual junction temperature at HTD condition (T_{vj_HTD}) which presents the baseline. For instance, at Test 1 $I_{C(tail)}$ is 15.88A at ITD conditions. The same $I_{C(tail)}$ at HTD condition, corresponding to the temperature T_{vj_HTD}=42.96°C. In Test 1 at ITD, T_{max}=$T_{j\text{-}Chip1}$=34.6°C, T_{mid}=$T_{j\text{-}Chip2}$=33°C, T_{min}=$T_{j\text{-}Chip3}$=30.8°C. Thus, T_{vj_HTD} - T_{max} = 8.36°C, T_{vj_HTD} - T_{mid} = 9.96°C, T_{vj_HTD} - T_{min} = 12.16°C. R3.7

R2.1

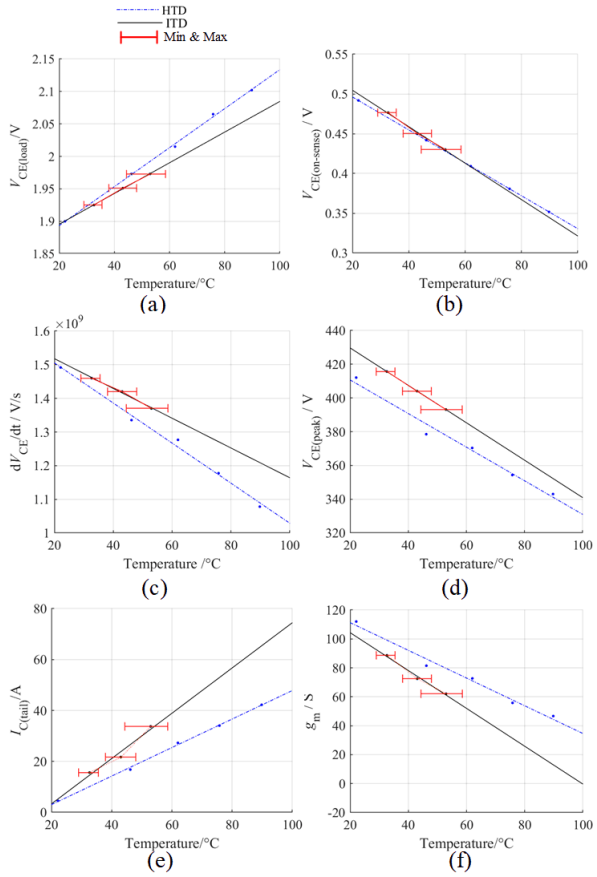

Fig. 20 Comparison of TSEPs versus T_{vj} between HTD and ITD conditions. (a) $V_{CE(on-load)}$. (b) $V_{CE(on-sense)}$. (c) dV_{CE}/dt. (d) $V_{CE(peak)}$. (e) $I_{C(tail)}$. (f) g_m. Min and max value in the red error bar indicate the coolest and hottest temperature of the switch.

TABLE V ACCURACY OF TSEPS (UNIT: °C)

TSEPs	No.	$T_{vj\ HTD}$ -T_{max}	$T_{vj\ HTD}$ -T_{mid}	$T_{vj\ HTD}$ -T_{min}
$V_{CE(on-load)}$	Test1	-4.12	-2.52	**-0.32**
	Test2	-6.42	-4.72	**-1.12**
	Test3	-10.42	-6.52	**-1.72**
$V_{CE(on-sense)}$	Test1	-5.16	**-3.56**	-1.36
	Test2	-3.54	**-1.84**	1.76
	Test3	-4.82	**-0.92**	3.88
dV_{CE}/dt	Test1	-7.08	-5.48	**-3.28**
	Test2	-11.38	-9.68	**-6.08**
	Test3	-14.18	-10.28	**-5.48**
$V_{CE(peak)}$	Test1	-19.60	-18.00	-15.80
	Test2	-19.06	-17.36	-13.76
	Test3	-19.22	-15.32	-10.52
g_m	Test1	9.00	10.60	12.80
	Test2	14.78	16.48	20.08
	Test3	14.46	18.36	23.16
$I_{C(tail)}$	Test1	8.36	9.96	12.16
	Test2	7.58	9.28	12.88
	Test3	17.9	21.8	26.6

R3.7

R1.2 R3.7 R3.8 Table V shows that all dynamic TSEPs have either only a positive or negative discrepancy. The largest inaccuracy is with $I_{C(tail)}$ for Test 3 and the best accuracy is with $V_{CE(on-sense)}$ at Test 1. Based on Fig. 20 and Table V the following can be concluded: $V_{CE(on-sense)}$ has good accuracy and provides a good agreement of T_{vj} between HTD and ITD. The reason for that is because the low sense current does not produce much heat to contribute to ITD. TSEPs $V_{CE(on-load)}$ and dV_{CE}/dt are measuring the chip that has the lowest temperature. TSEP $V_{CE(peak)}$ predicts a temperature that is well below the lowest chip temperature and TSEPs g_m and $I_{C(tail)}$ predict values well above the hottest chip temperature.

R1.2 The reasoning that TESPs track either the hottest or coldest chip temperatures is due to the discrepancy of T_{vj} at ITD from T_{vj} at HTD as indicated in Fig. 20. At ITD, temperatures for each chip differ. Consequently, the switching and conduction performance of each chip differ too. Changes in the semiconductor performance between IGBT chips cause current redistribution and leads to consistent shifts in the turn-on and turn-off characteristics of the IGBT switch as shown in Fig.21 and Fig.22.

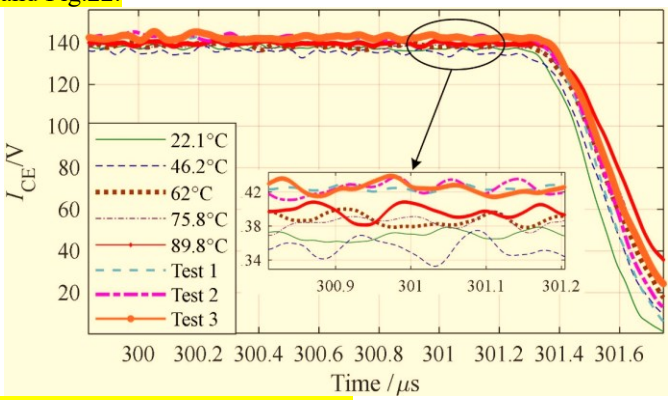

Fig. 21. Shifts in I_C during the first pulse.

R1.2 Fig. 21 depicts I_C during the first pulse. It can be noticed that the on-state current I_C of tests at the ITD condition is higher than that at the HTD condition. The current rise is caused by the reduction of the equivalent on-state resistance of the IGBT switch. On the one hand, at the same temperature, this will lead to a lower $V_{CE(on-load)}$ at ITD conditions compared with HTD. Thus, according to the baseline at HTD, the prediction from $V_{CE(on-load)}$ is lower than T_{vj} at ITD. On the other hand, at the same temperature, a higher on-state current means a higher tail current during the turn-off transient. As a result, according to the baseline at HTD, the prediction from $I_{C(tail)}$ is higher than T_{vj} at ITD. Furthermore, due to the imbalance current distribution between three chips at ITD, the current slope depends on the slowest one which leads to a smaller g_m at ITD conditions. Subsequently, according to the baseline at HTD, the prediction from g_m is higher than T_{vj} at ITD.

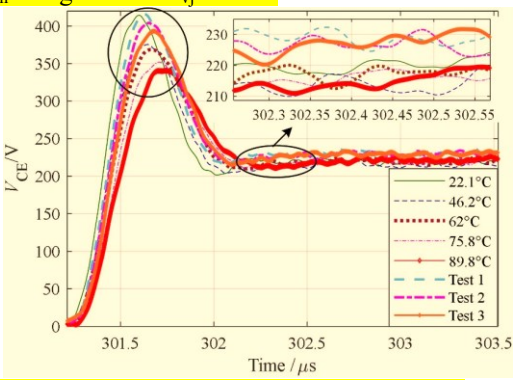

Fig. 22. Shifts in V_{CE} at off-state captured during the first pulse.

R1.2 A similar phenomenon is also captured in V_{CE} as shown in Fig. 22. During turn-off transient, V_{CE} overshoot is higher at ITD conditions than that at HTD conditions. This also means

the voltage stress is higher. At the same temperature condition, this means a larger $V_{CE(peak)}$ and steeper dV_{CE}/dt during the turn-off transient at ITD compared to HTD conditions. Hence, according to the baseline at HTD, the predictions from dV_{CE}/dt and $V_{CE(peak)}$ are lower than T_{vj}.

TABLE VI SENSITIVITY OF TSEPs

	TSEPs	Sensitivity(/°C)	Linearity
On state	$V_{CE(on\text{-}load)}$	2.400 mV ↑	0.9981
	$V_{CE(on\text{-}sense)}$	2.300 mV ↓	0.9958
	dV_{CE}/dt	4.000 V/µs ↓	0.9989
Turn off	$V_{CE(peak)}$	1.110 V ↓	0.9987
	g_m	1.309 S ↓	0.9882
	$I_{C(tail)}$	0.889 A ↑	0.9611

Table VI compares the sensitivity and the linearity based on (2) and (3). Table VI concludes that all TSEPs show good linearity at ITD conditions and values do not differ dramatically from the linearity values shown at HTD. Sensitivity, however, varies slightly. The sensitivity for all dynamic TSEPs increases at ITD. The sensitivity for the static TSEP $V_{CE(on\text{-}sense)}$ also increases whereas the sensitivity for $V_{CE(on\text{-}load)}$ decreases during ITD operation. However, the difference in sensitivity for each TSEP at HTD and ITD is small. Consequently, one can conclude that at ITD condition, all TSEPs under investigation demonstrate reasonable linearity and sensitivity.

VI. CONCLUSIONS

This paper has explored the relationship between TSEPs and the global virtual temperature T_{vj} in mIGBT power modules.

Ten conventional TSEPs, static and dynamic, were selected and measured on an mIGBT power module operating at both homogeneous temperature distribution (HTD) and inhomogeneous temperature distribution (ITD) conditions. TSEPs and temperatures were both recorded (and/or derived) for HTD and ITD conditions. TSEPs' ability to track the hottest or coldest temperatures, their linearity, and sensitivities were quantitively compared. Results show that TSEPs provide good linearity at both HTD and ITD. Also, sensitivity is less influenced when operating at ITD. Of all TSEPs under investigation, $V_{CE(on\text{-}sense)}$ is the most accurate TSEP for HTD and ITD conditions. In the future, more research should be carried out regarding the influence of operating conditions on TSEPs' performance at ITD conditions. R2.2

VII. ACKNOWLEDGEMENT

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REFERENCES

[1] V. I. Smirnov, V. A. Sergeev, A. A. Gavrikov, and A. M. Shorin, "Thermal Impedance Meter for Power mosfet and IGBT Transistors," *IEEE Transactions on Power Electronics,* vol. 33, no. 7, pp. 6211-6216, 2018, doi: 10.1109/TPEL.2017.2740961.

[2] B. Ji *et al.*, "In Situ Diagnostics and Prognostics of Solder Fatigue in IGBT Modules for Electric Vehicle Drives," *IEEE Transactions on Power Electronics,* vol. 30, no. 3, pp. 1535-1543, 2015, doi: 10.1109/TPEL.2014.2318991.

[3] E. Wolfgang, "Examples for failures in power electronics systems," presented at the ECPE Tutorial on Reliability of Power Electronic Systems, Nuremberg, Germany, Apr. 2007, 2007.

[4] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters-A Review," *Power Electronics, IEEE Transactions on,* vol. 27, no. 6, pp. 3081-3092, 2012, doi: 10.1109/TPEL.2011.2178433.

[5] Infineon. "Technical Information IGBT Modules Definition and use of junction temperature values." (accessed AN2008-01.

[6] H. P. S. D. Ltd., "Junction Temperature Definitions," 2015.05.29. '15 LD-ES-130737-R1.

[7] P. Jacob, M. Held, P. Scacco, and W. Wuchen, "Reliability testing and analysis of IGBT power semiconductor modules," in *IEE Colloquium on IGBT Propulsion Drives*, 25 Apr 1995 1995, pp. 4/1-4/5, doi: 10.1049/ic:19950531.

[8] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, 26-29 May 1997 1997, vol. 1, pp. 425-430 vol.1, doi: 10.1109/PEDS.1997.618742. [Online]. Available: http://ieeexplore.ieee.org/ielx3/4887/13474/00618742.pdf?tp=&arnumber=618742&isnumber=13474

[9] B. Ji, "In-situ Health Monitoring of IGBT Power Modules in EV Applications," Ph.D., School of Electrical and Electronic Engineering, Newcastle University, Newcastle University, 2011.

[10] L. Dupont and Y. Avenas, "Evaluation of thermo-sensitive electrical parameters based on the forward voltage for on-line chip temperature measurements of IGBT devices," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 14-18 Sept. 2014 2014, pp. 4028-4035, doi: 10.1109/ECCE.2014.6953950. [Online]. Available: http://ieeexplore.ieee.org/ielx7/6926643/6953358/06953950.pdf?tp=&arnumber=6953950&isnumber=6953358

[11] M. Denk and M.-M. Bakran, "An IGBT Driver Concept with Integrated Real-Time Junction Temperature Measurement," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, 20-22 May 2014 2014, pp. 1-8.

[12] N. Baker, S. Munk-Nielsen, F. Iannuzzo, L. Dupont, and M. Liserre, "Experimental evaluation of IGBT junction temperature measurement via peak gate current," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, 8-10 Sept. 2015 2015, pp. 1-11, doi: 10.1109/EPE.2015.7311733.

[13] M. Denk and M. M. Bakran, "Comparison of UCE and RGi based junction temperature measurement of multichip IGBT power modules," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 8-10 Sept. 2015 2015, pp. 1-11, doi: 10.1109/EPE.2015.7309067.

[14] N. Baker, F. Iannuzzo, S. Munk-Nielsen, L. Dupont, and Y. Avenas, "Experimental Evaluation of IGBT Junction Temperature Measurement via a Modified-VCE(deltVCE_deltVGE) Method with Series Resistance Removal," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 8-10 March 2016 2016, pp. 1-6.

[15] X. Zhuxian, X. Fan, and W. Fei, "Junction Temperature Measurement of IGBTs Using Short-Circuit Current as a Temperature-Sensitive Electrical Parameter for Converter Prototype Evaluation," *Industrial Electronics, IEEE Transactions on,* vol. 62, no. 6, pp. 3419-3429, 2015, doi: 10.1109/TIE.2014.2374575.

[16] A. Ammous, B. Allard, and H. Morel, "Transient temperature measurements and modeling of IGBT's under short circuit," *IEEE Transactions on Power Electronics,* vol. 13, no. 1, pp. 12-25, 1998, doi: 10.1109/63.654955.

[17] Z. Jakopovic, Z. Bencic, and F. Kolonic, "Important properties of transient thermal impedance for MOS-gated power semiconductors," in *ISIE '99. Proceedings of the IEEE International Symposium on Industrial Electronics (Cat. No.99TH8465)*, 12-16

July 1999 1999, vol. 2, pp. 574-578 vol.2, doi: 10.1109/ISIE.1999.798675.

[18] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-Time Temperature Estimation for Power MOSFETs Considering Thermal Aging Effects," *IEEE Transactions on Device and Materials Reliability,* vol. 14, no. 1, pp. 220-228, 2014, doi: 10.1109/TDMR.2013.2292547.

[19] H. Niu and R. D. Lorenz, "Sensing IGBT junction temperature using gate drive output transient properties," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 15-19 March 2015 2015, pp. 2492-2499, doi: 10.1109/APEC.2015.7104700. [Online]. Available: http://ieeexplore.ieee.org/ielx7/7097563/7104313/07104700.pdf?tp=&arnumber=7104700&isnumber=7104313

[20] H. Kuhn and A. Mertens, "On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 8-10 Sept. 2009 2009, pp. 1-10.

[21] J. A. Butron Ccoa, B. Strauss, G. Mitic, and A. Lindemann, "Investigation of Temperature Sensitive Electrical Parameters for Power Semiconductors (IGBT) in Real-Time Applications," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, 20-22 May 2014 2014, pp. 1-9.

[22] A. Bryant *et al.*, "Investigation Into IGBT dV/dt During Turn-Off and Its Temperature Dependence," *IEEE Transactions on Power Electronics,* vol. 26, no. 10, pp. 3019-3031, 2011, doi: 10.1109/TPEL.2011.2125803.

[23] N. Baker, S. Munk-Nielsen, M. Liserre, and F. Iannuzzo, "Online junction temperature measurement via internal gate resistance during turn-on," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 26-28 Aug. 2014 2014, pp. 1-10, doi: 10.1109/EPE.2014.6911024. [Online]. Available: http://ieeexplore.ieee.org/ielx7/6898115/6910682/06911024.pdf?tp=&arnumber=6911024&isnumber=6910682

[24] V. Sundaramoorthy, E. Bianda, R. Bloch, I. Nistor, G. Knapp, and A. Heinemann, "Online estimation of IGBT junction temperature (Tj) using gate-emitter voltage (Vge) at turn-off," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2-6 Sept. 2013 2013, pp. 1-10, doi: 10.1109/EPE.2013.6634444. [Online]. Available: http://ieeexplore.ieee.org/ielx7/6611296/6631728/06634444.pdf?tp=&arnumber=6634444&isnumber=6631728

[25] D. Barlini, M. Ciappa, A. Castellazzi, M. Mermet-Guyennet, and W. Fichtner, "New technique for the measurement of the static and of the transient junction temperature in IGBT devices under operating conditions," *Microelectronics Reliability,* vol. 46, no. 9–11, pp. 1772-1777, 9// 2006.

[26] H. Luo, W. Li, F. Iannuzzo, X. He, and F. Blaabjerg, "Enabling Junction Temperature Estimation via Collector-Side Thermo-Sensitive Electrical Parameters Through Emitter Stray Inductance in High-Power IGBT Modules," *IEEE Transactions on Industrial Electronics,* vol. 65, no. 6, pp. 4724-4738, 2018, doi: 10.1109/TIE.2017.2745442.

[27] R. Mandeya, C. Chen, V. Pickert, and R. T. Naayagi, "Prethreshold Voltage as a Low-Component Count Temperature Sensitive Electrical Parameter Without Self-Heating," *IEEE Transactions on Power Electronics,* vol. 33, no. 4, pp. 2787-2791, 2018, doi: 10.1109/TPEL.2017.2749179.

[28] F. Carastro, M. Bland, A. Castellazzi, J. C. Clare, C. M. Johnson, and P. W. Wheeler, "Investigation of the electro-thermal stress affecting IGBT modules in high-pulsed power resonant converters," in *2009 IET European Pulsed Power Conference*, 21-25 Sept. 2009 2009, pp. 1-4, doi: 10.1049/cp.2009.1670.

[29] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Springer Science+Business Media, 2008, p. 1069.

[30] M. Trivedi and K. Shenai, "Modeling IGBT turn-off in hard- and soft-switching applications," in *Proceedings of APEC 97 - Applied Power Electronics Conference*, 27-27 Feb. 1997 1997, vol. 1, pp. 156-160 vol.1, doi: 10.1109/APEC.1997.581447.

[31] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction Temperature Extraction Approach With Turn-Off Delay Time for High-Voltage High-Power IGBT Modules," *IEEE Transactions on Power Electronics,* vol. 31, no. 7, pp. 5122-5132, 2016, doi: 10.1109/TPEL.2015.2481465.

[32] X. Dewei, L. Haiwei, H. Lipei, S. Azuma, M. Kimata, and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices," in *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE*, 1999 1999, vol. 1, pp. 729-734 vol.1, doi: 10.1109/IAS.1999.800030. [Online]. Available: http://ieeexplore.ieee.org/ielx5/6470/17346/00800030.pdf?tp=&arnumber=800030&isnumber=17346

[33] X. Dewei, L. Haiwei, H. Lipei, S. Azuma, M. Kimata, and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices," *IEEE Transactions on Industry Applications,* vol. 38, no. 5, pp. 1426-1431, 2002, doi: 10.1109/TIA.2002.802995.

[34] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction Temperature Extraction Approach with Turn-off Delay Time for High-voltage High-Power IGBT Modules," *IEEE Transactions on Power Electronics,* pp. 1-1, 2015, doi: 10.1109/tpel.2015.2481465.

[35] J. B. Witcher, "Methodology for Switching Characterization of Power Devices and Modules," Master, Electrical Engineering, Faculty of Virginia Polytechnic Institute and State University https://vtechworks.lib.vt.edu/bitstream/handle/10919/31205/thesis.pdf?sequence=1&isAllowed=y, 2002.