In Situ Diagnosis of Wire Bonding Faults for Multichip IGBT Modules Based on the Crosstalk Effect

Wuyu Zhang, Kun Tan, *Member, IEEE,* Bing Ji, *Senior Member, IEEE,* Lei Qi, Xiang Cui, *Senior Member, IEEE,* Jixuan Wei, and Xiangyu Zhang

***Abstract*—Introducing bond wire diagnosis for multichip IGBT modules is key to the health monitoring of modular multilevel converters (MMCs), which allows for improved field robustness, reliability, and reduced maintenance cost. This paper leverages the crosstalk phenomenon during switching transitions to detect the chip open-circuit faults caused by the bond wire lift-off using typical half-bridge IGBT modules in a multichip-parallel configuration. The cycle-controlled, non-intrusive measurement is conducted under normal operation, when the device under test is at off-state and its complementary switch is during switching transitions. Two specialized health sensitive parameters arising from the dynamic gate loop waveforms are identified and evaluated, including 1) the gate voltage $V_{GE(t3)}$ when the declining collector voltage reaches zero, and 2) the negative peak gate voltage $V_{GE(t4)}$. The sensitivity and stability of these two parameters are compared through theoretical analysis, circuit simulation and practical verification. The results show that $V_{GE(t4)}$ is more suitable for online monitoring, while $V_{GE(t3)}$ is more sensitive than $V_{GE(t4)}$. With managed complexity in gate drives, this proposed health awareness approach is feasible in the submodules of MMC applications, but it can also be used in other power converter topologies incorporating the half-bridge structure.**

***Index Terms*—Multichip insulated gate bipolar transistor (IGBT) module, Bond wires diagnosis, Crosstalk phenomenon, Modular multilevel converter (MMC)**

I. Introduction

Modular multilevel converter (MMC) has the advantages of modular expansion capability, excellent harmonic performance and low loss, which is widely used in high-voltage direct current (HVDC) transmission systems [1], [2]. MMC is a large and complex system with hundreds or thousands of submodules (SMs), and each submodule is composed of IGBT modules, capacitors, control unit and water-cooled heat sink, etc. A SM commonly contains power devices configured as the half-bridge structure as shown in Fig.1. The half-bridge submodules MMC has been already applied in commercial DC transmission projects, such as, Nemo link [3], Nan'ao three-terminal DC project [4], and Zhoushan five-terminal DC project [5]. Due to the harsh operating conditions and large amount of components utilized in the MMC than other converter topologies, its reliability has become the bottleneck of further application [6]. IGBT module is the core component forming the SM in the MMC, hence its failure results in loss of function of the SM. Due to the existence of the redundant module, the MMC will not immediately fail and stop the operation. The redundant submodules realize the protection of the system and is a protection method after the failure of the IGBT module. The health monitoring of the IGBT module is the diagnosis before failure and provides the additional aging information of the entire MMC. The application of aging information can guide MMC's power outage maintenance time and design rotation control to achieve the long-term stress balance of each submodule. The health monitoring of the IGBT modules and the redundancy of the submodules can upgrade the protection of MMC and improve its reliability.

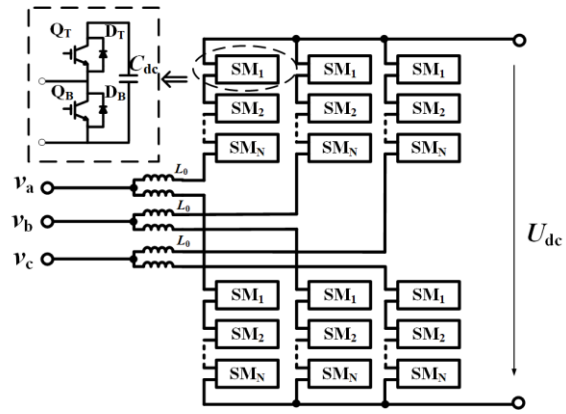

Fig. 1 Circuit structure of an MMC and its submodule

The high-power IGBT modules always consist of multiple IGBT and diode chips, which are connected in parallel to enhance the current carrying capability, referred to as the multichip IGBT modules [7], [8]. In the multichip IGBT modules, compared with diode chip, IGBT chip has more complex structure and bears greater stress in turn-on and turn off process, which leads to lower reliability. Aluminum wires are bonded in the IGBT module for electrical interconnections. The bond wire fatigue is one of the main failure modes of IGBT modules [9], [10]. Under the thermal shock caused by power dissipation of IGBT chip in operating, due to the large difference of thermal expansion coefficient of materials, the

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most common failure mode of bond wires is that the emitter aluminum bond wires lifts off from the surface of IGBT chip.

For an IGBT chip, several bond wires are connected to its top emitter metallisation, providing the electrical connection to the external power loop. As the bond wires fatigue and the lift-off failure mode progresses, the electrical connectivity of the associated chip deteriorates. If all bond wires connected to the chip are subject to the lift-off failure, the ultimate loss of electrical connection to power loop is established, resulting in a chip open circuit fault, which can be treated as the pertinent virtual chip failure. Thanks to the redundant feature in the typical module design using multiple chips in a paralleled connection, the open-circuit failure in a single chip might not propagate straightaway to lead to the ultimate power module within a short period of time [11]. However, the long-term robustness of whole IGBT module depends on each of the constitutive chips [12], [13]. In this regard, IGBT chip open is the condition monitoring precursor for multichip IGBT modules. Attention must be paid to the precursory diagnosing and adaptively protecting of modules with bond wires failure .

Bond wires fatigue will not only change the resistance and stray inductance in the circuit, but also change the capacitance distribution. Much research on condition monitoring of bond wires failure has been reported in recent years. From the perspective of monitoring signal, it can be divided into electrical quantity and nonelectrical quantity, the nonelectric quantity monitoring method needs special measuring device [14], [15], which is difficult to be applied in online monitoring. The essence of electrical quantity monitoring method is the identification of circuit parameters, that is, the change of characteristic electrical quantity reflects the change of circuit parameters caused by bond wires failure. Apparently, the larger the excitation source of circuit, the higher identification accuracy is obtained.

Considering the position of the electrical quantity monitored, monitoring can be taken at either the power loop (emitter-collector) or the gate loop (gate-emitter, gate-kelvin emitter). The electrical parameters can be monitored from the power loop circuit mainly include: saturation voltage $V_{CE(SAT)}$ [16]-[18], short circuit current [19], on-state resistance [20],[21] and turn off time t_{off} [22], [23], *et al*. In the process of monitoring, by using load current or capacitor voltage as the excitation source to identify circuit parameters, higher identification accuracy and less intrusive measurement can be achieved, so they are widely used, especially used in the monitoring condition of part of the bond wire fatigue of the IGBT chip. However, such characteristic quantities are more sensitive to load current and junction temperature fluctuations, and usually require an accurate information of current and junction temperature during the process of monitoring. The monitoring device and circuit need to be isolated from the high voltage in power loop.

The electrical parameters can be monitored from the gate loop circuit mainly include: the threshold voltage [24], the gate peak current [25], the Miller platform voltage [26], [27], and the gate charging time [13], *et al*. In the process of monitoring, the driving voltage is used as the excitation source of circuit parameter identification, which is only tens of volts. It is easy to be affected by the measurement noise. It is usually used in the monitoring condition of the IGBT chip open, and is not easily affected by load current and junction temperature fluctuations. The monitoring device is easy to integrate into the gate drive unit of the IGBT module.

For a half-bridge structure such as those found in the submodules of MMC, as shown in Fig.1, the gate voltage spike signals manifest themselves at the off-state switch due to the so-called crosstalk phenomenon, when the turn-on or turn-off transition takes place at its complementary device [28]-[31]. This has provided a unique opportunity for in-situ health monitoring of wire bonding faults.

In this paper, a monitoring method for IGBT chip open fault caused by the entire loss of related emitter bond wires in a multichip IGBT module is proposed. It is realized by measuring the gate voltage of the off-state IGBT switch based on the crosstalk phenomenon during the turn off process of a complementary switch. It offers cycle-by-cycle measurement, high sensitivity and simplicity in sensing and readout circuit design without significant intrusiveness to converter design and operation. The proposed method combines the advantages of monitoring from the gate loop by avoiding large voltage steps and taking large changing signals from the power loop as stimulus. The collector voltage slope is used as the stimulus for circuit status identification. It is also less susceptible to interference caused by chip temperature variations or high current transients (di_c/dt) appearing in operational converters. Although the method is proposed for the IGBT submodule in the MMC applications, it is also applicable to other power electronic converters incorporating the half-bridge structure of two active switches.

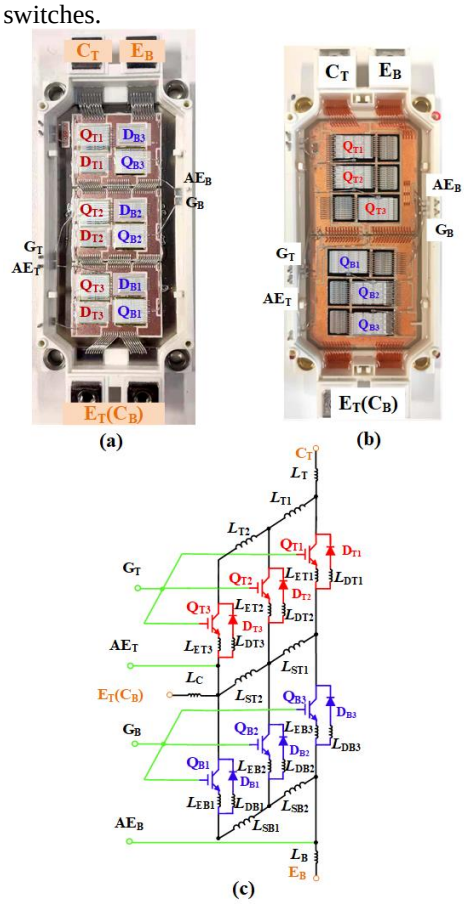


Fig. 2 The IGBT open modules under test including (a) TXFF450R120MC1 and (b) FF600R17ME4 and (c) the equivalent circuit of TXFF450R120MC1.

II. Mechanism of the Monitoring Method

A. Crosstalk phenomenon of IGBT module

Two multichip IGBT open modules from different manufacturers of TAIXIN's IGBT module (TXFF450RMC1) and Infineon (FF600R17ME4) are used as the device-under-test in this paper and their internal structures are shown in Fig.2. Both are configured in a half-bridge structure consisting of one upper switch and one lower switch in the phase-leg and each switch incorporates three IGBT chips and three freewheeling diode chips connected in parallel. The IGBT's collector and the diode's cathode are electrically connected to the copper plane on the surface of substrate through solder, while the emitter and anode are connected via aluminum bond wires. Fig.2(c) shows the equivalent circuit of TXFF450RMC1, which is focused in the crosstalk instrumentation experiment. L_{ETi} and L_{EBi} (i=1, 2, 3) are the stray inductance of the bond wires between the emitter of the IGBT chip and the substrate; L_{DTi} and L_{DBi} (i=1, 2, 3) are the stray inductance of the bond wires between the anode of the diode chip and the substrate, where the letters T and B refer to the top and bottom devices respectively. The stray inductance of a single bonding wire is about 15nH [25], thus the total inductance of L_{ETi}, L_{EBi}, L_{DTi},and L_{DBi} could be negligible as multiple wires are usually connected in parallel, which has 8 wires for each chip in this case. The stray inductance L_{STi} and L_{SBi} (i=1, 2) are composed of the equivalent inductance of the copper plane of substrate and the bond wires between the parallel-connected chips. Their inductance is greater than those emitter and anode bonding wires, and should be noticed that they are both existing in the power loop and the gate loop, which have greater impact on the crosstalk phenomenon.

A double-pulse test circuit diagram is shown in Fig.3 (a) to illustrate the crosstalk phenomenon in a half-bridge module. The top IGBT Q_T is switched normally, while the bottom IGBT Q_B is in the off-state. The gate voltage v_{GEB} is measured between the gate (G) and the auxiliary emitter (AE) terminals of Q_B.

The crosstalk occurs under two typical scenarios [31]: (1) the change of collector-emitter voltage v_{CEB} on Q_B caused by the active switching of Q_T leads to charging or discharging of the gate collector capacitance C_{GCB}. Its capacitive current flows through the gate resistor to produce a voltage drop opposite to the gate voltage V_{GB} of Q_B; as shown in the t_2-t_3 stage of Fig.3 (b), (2) Due to the current commutation, a voltage on the common emitter inductance of the gate loop and the power loop L_{SB} will be induced, which can also influence the gate voltage of Q_B, as shown in the t_3-t_5 stage of Fig.3 (b).

B. The effect of IGBT bond wires failure in t_2-t_3 stage

Fig.3 (b) shows the typical switching waveforms during the turn-off transition of Q_T, while Q_B is kept off by a negative gate voltage. A negative voltage overshoot will be generated on v_{GEB} of the bottom IGBT Q_B. The solid curve of v_{GEB} represents the behavior of a healthy IGBT module, which is referred as "baseline". The dashed curve describes v_{GEB} of a faulty module with all bond wires on a chip failed, which is referred as "bond wires failure" in the following discussion.

During the t_2-t_3 stage, the gate voltage v_{GET} of the Q_T is clamped on the Miller platform, and the Miller capacitor C_{GCT} is charged. The collector-emitter voltage v_{CET} of the Q_T

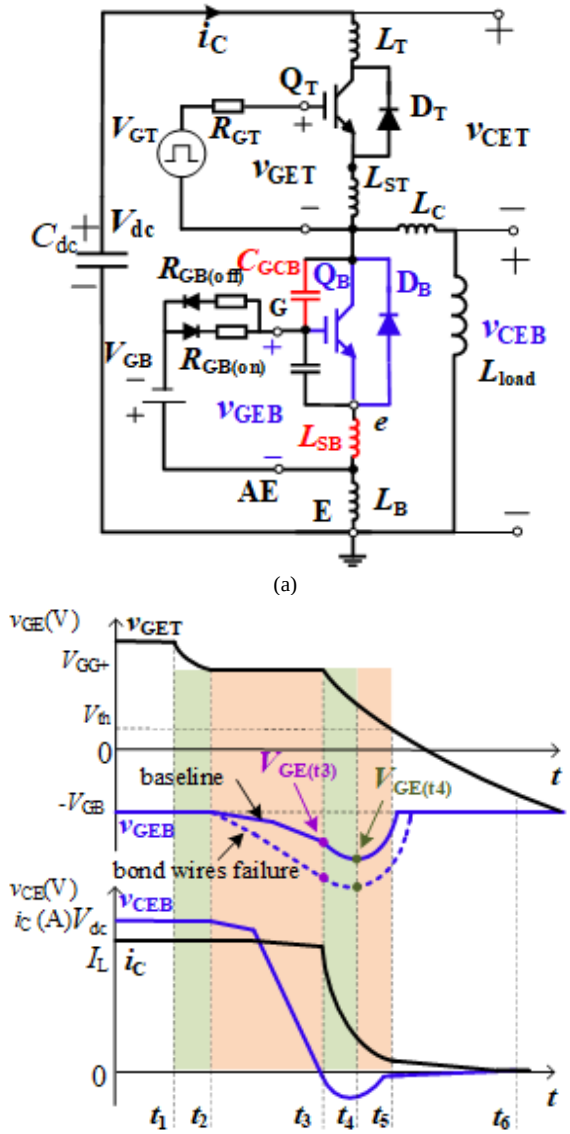


Fig.3 (a) A double-pulse experimental circuit for crosstalk analysis and IGBT bond wires failure tests (b)Analysis waveform of v_{GEB}

gradually increases, correspondingly, v_{CEB} of the Q_B decreases.

The bottom diode D_B is reverse biased and not conducting. Since the collector current i_C remains unchanged before the current commutation starts, the voltage rate of both transistors can be found below:

$$\frac{dv_{CEB}}{dt} = -\frac{dv_{CET}}{dt} \tag{1}$$

The Miller capacitor C_{GCB} of the Q_B is discharged, and its current i_{GCB} flows through the gate resistor $R_{GB(on)}$, resulting in a voltage drop negatively superimposed on the gate supply voltage $-V_{GB}$ and thus an undershoot of gate voltage appearing on v_{GEB}, as show in Fig4. (a).

For the effect of bond wires failure, the IGBT Q_{B2} branch of the Q_B is taken as an example. The capacitance current distribution before the bond wires failure is shown in Fig.4 (b). The capacitance C_{GCB2} discharged current i_{GCB2} is composed of the gate current i_{G2} and the C_{GEB2} discharge current. Ignoring

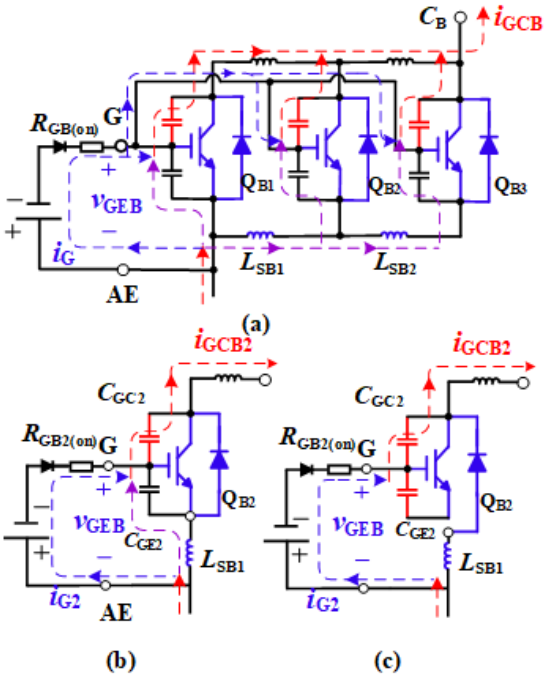


Fig. 4 Equivalent circuit in t_2-t_3 process. (a) IGBT in baseline state, (b) the branch equivalent circuit of IGBT Q_{B2} in baseline state, (c) the branch equivalent circuit of bond wires failure.

the stray inductance voltage in the loop, and dv_{CEB}/dt is simplified to constant -k, v_{GEB} is:

$$\frac{dv_{CEB}}{dt} = -k \tag{2}$$

$$v_{GEB} = -kR_{GB2(on)}C_{GCB2}(1-e^{-t/\tau_1}) - V_{GB} \tag{3}$$

The time constant $\tau_1 = R_{GB2(off)}(C_{GCB2}+C_{GEB2})$, v_{GEB} decreases during t_2-t_3 stage, and the gate voltage v_{GEB} at t_3 is defined as:

$$v_{GEB}(t_3) = V_{GE(t3)} \tag{4}$$

The IGBT Q_{B2} emitter open circuit, which caused by all bond wires fatigue, leads to the gate-emitter capacitance C_{GEB2} disconnected from the power loop, as shown in Fig. 4 (c). The distribution of the capacitance current i_{GCB2} changes and i_{GCB2} only flows through the gate resistance v_{GEB} decreases compared to its value in baseline state at the same time, and $V_{GE(t3)}$ decreases correspondingly.

C. *The effect of IGBT bond wires failure in t_3-t_5 stage*

During the t_3-t_5 stage, as show in Fig.5 (a), at t_3, v_{CEB} of the Q_B drops to zero, and anti-parallel diode D_B begins to conduct. The load current begins to commutate from Q_T to the D_B, and the diode current i_{DB} satisfies the relationship with i_C:

$$-\frac{di_C}{dt} = \frac{di_{DB}}{dt} \tag{5}$$

i_{DB} flowing through the coupled inductor L_{SBi} generates the induced voltage v_{Ls}. In order to make the analysis clearer, taking the IGBT Q_{B2} branch as an example, as shown in Fig.5(b). At t_3(0-), v_{GEB} is $V_{GE(t3)}$, ignoring the loop stray inductance voltage at t_3(0-), and v_{Ge} is:

$$v_{Ge}\big|_{t=t_3} = V_{GE(t3)} \tag{6}$$

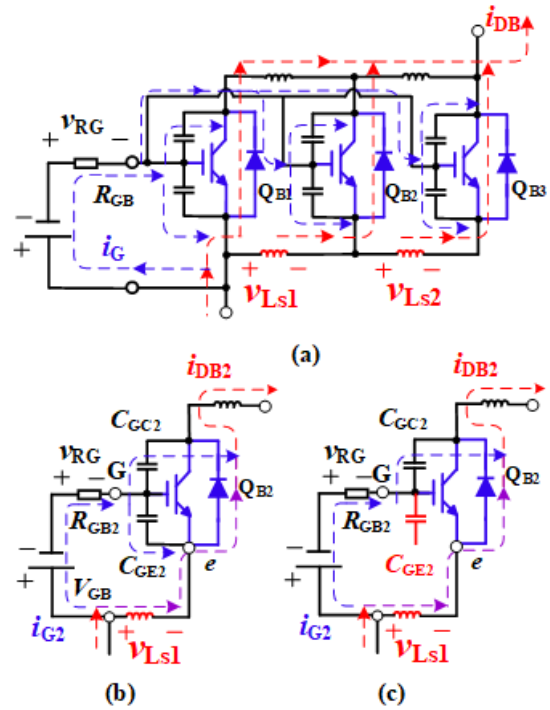


Fig.5 Equivalent circuit in t_3-t_5 process. (a) IGBT in healthy state, (b) the branch equivalent circuit of IGBT Q_{B3} in healthy state, (c) the branch equivalent circuit of bond wires failure.

At t_3(0+), the load current starts to transfer the diode D_B. The capacitors C_{GCB2} and C_{GEB2} are charged by the gate resistor $R_{GB(on)}$, and the KVL equation of the gate loop is given:

$$R_{GB2(off)}(C_{GC2}+C_{GE2})\frac{dv_{Ge}}{dt} + v_{Ge} = v_{LS1} - V_{GB} \tag{7}$$

Combined with the initial conditions (4), v_{Ge} can be obtained by solving:

$$v_{Ge} = \left(V_{GE(t3)} - v_{LS1} - V_{GB}\right)e^{-(t-t_3)/\tau_2} + v_{LS1} - V_{GB} \tag{8}$$

The gate voltage v_{GEB} during t_3-t_5 stage is:

$$\begin{aligned} v_{GEB} &= v_{Ge} - v_{LS1} \\ &= \left(V_{GE(t3)} - v_{LS1} + V_{GB}\right)e^{-(t-t_3)/\tau_2} - V_{GB} \end{aligned} \tag{9}$$

The time constant $\tau_2 = R_{GB2}(C_{GCB2}+C_{GEB2})$, v_{LS1} is:

$$v_{LS1} = L_{SB1}\frac{di_{DB2}}{dt} \tag{10}$$

In the initial stage of current transfer, t_3-t_4 stage, di_{DB2}/dt continues to increase and v_{LS1} increases. v_{GEB} decreases accordingly, and reaches its negative peak at t_4. t_3-t_4 stage, di_{DB2}/dt decrease and v_{LS1} decreases. v_{GEB} increases accordingly. The negative peak voltage of the gate voltage v_{GEB} at t4 is defined as:

$$v_{GEB}(t_4) = V_{GE(t4)} \tag{11}$$

It can be seen that $V_{GE(t4)}$ is the result of the combined effects of t_2-t_3 and t_3-t_4 stages. $V_{GE(t4)}$ can be expressed as:

$$V_{GE(pk)} = V_{GE(t3)} - |\Delta V_{GE}| \tag{12}$$

ΔV_{GE} is the effect of t_3-t_4 stage.

After the IGBT Q_{B2} failure caused by all bond wires fatigue,

the gate-emitter capacitance C_{GEB2} is disconnected from the gate loop, as shown in Fig.5(c). $V_{GE(t3)}$ decreases, and the time constant τ_2 decreases. v_{GEB} decreases compared to its value in baseline state at the same time, and $V_{GE(t4)}$ decreases correspondingly.

According to the analysis of the turn off process, the gate voltage v_{GEB} decreases gradually from t_2 to t_4 and reaches the negative peak at t_4, the impact of bond wires failure on v_{GEB} is divided into t_2-t_3 and t_3-t_4 stages. During the turn off process, the gate voltage v_{GEB} has two typical values that can reflect the bond wires failure: 1) the gate voltage $V_{GE(t3)}$ at the time of the two-stage boundary, 2) negative voltage peak value of gate voltage $V_{GE(t4)}$. Bond wires failure causes $V_{GE(t3)}$ and $V_{GE(t4)}$ to decrease compared to their values before failure. Therefore, experiments will be carried out to compare the sensitivity and stability of $V_{GE(t3)}$ and $V_{GE(t4)}$ in monitoring IGBT bond wires failure.

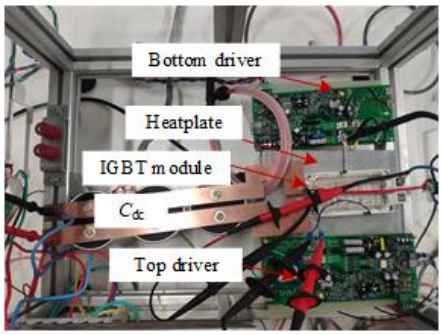


Fig.6 Photograph of experimental platform.

TABLE I
PLATFORM PARAMETERS OF EXPERIMENTAL PLATFORM

Parameters	Value
C_{dc}	1.2mF
L_s	0.3mH
R_{GT}	2.2Ω
$R_{GB(on)}$	5.3Ω、24Ω、75Ω
$R_{GB(off)}$	2.2Ω
V_{GB}	-6.45V

III. Experimental Validation

The experimental platform is shown in Fig.6, and its circuit schematic is same as Fig.3 (a). The load inductance L_{load} is connected in parallel with the bottom IGBT Q_B. The top IGBT Q_T is in the normal turning on and off state, and the Q_B maintains negative pressure shutdown state. The relevant parameters of the experimental platform are shown in TABLE I. It should be noticed that when Q_T is turning on, the increasing v_{CEB} of Q_B will charge the Miller capacitor C_{GCB}, hence the induced current flowing through $R_{GB(off)}$ and C_{GEB} might cause the faulty parasitic turn-on of Q_B. To avoid this fault, a small turn-off gate resistance $R_{GB(off)}$ is selected.

Bond wires failure on the IGBT Q_{B2} is emulated by cutting off all the eight emitter bond wires. Fig.7(a) compares the changes of $V_{GE(t3)}$ and $V_{GE(t4)}$ after the bond wires failure occurs in Q_{B2} at 20°C of the TXFF450RMC1. The load current I_L is 100A, and $R_{GB(on)}$ is 75Ω. It can be seen that $V_{GE(t3)}$ and $V_{GE(t4)}$ decrease to more negative values after bond wires failure occurred, and both of them can be used as the failure-sensitive

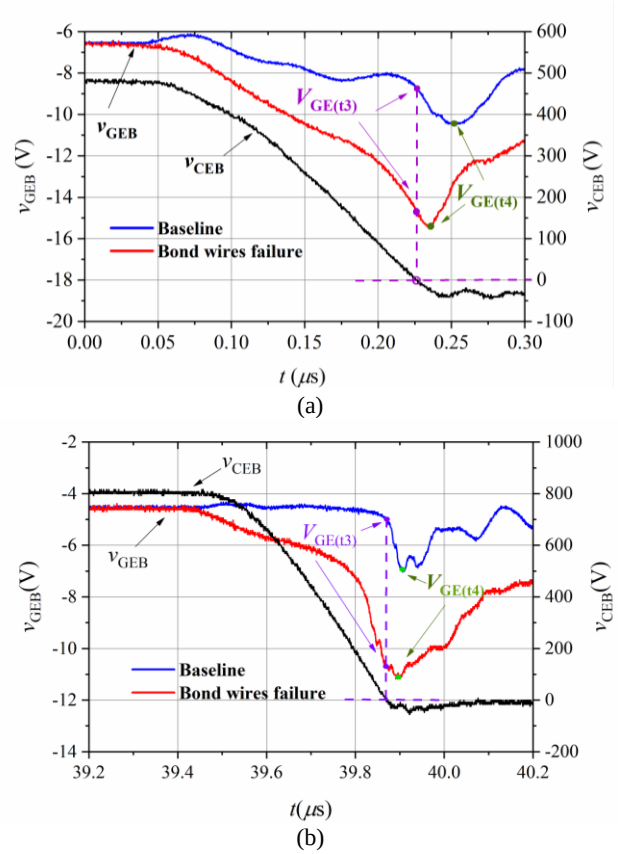


Fig.7 $V_{GE(t3)}$ and $V_{GE(t4)}$ changes with bond wires failure at 20°C. (a) The result of TXFF450RMC1. (b) The result of FF600R17ME4

parameters for monitoring. $V_{GE(t3)}$ is decreased from -8.62V to -14.57V with a variation of 5.95V, $V_{GE(t4)}$ is decreased from -10.35V to -15.42V with a variation of 5.07V. Considering the t_3-t_4 stages in $v_{GEB\_baseline}$ and $v_{GEB\_bond\ wires\ failure}$ respectively, $|\Delta V_{GE}|$ is decreased from 1.73V to 0.85V, with a variation of 0.88V.

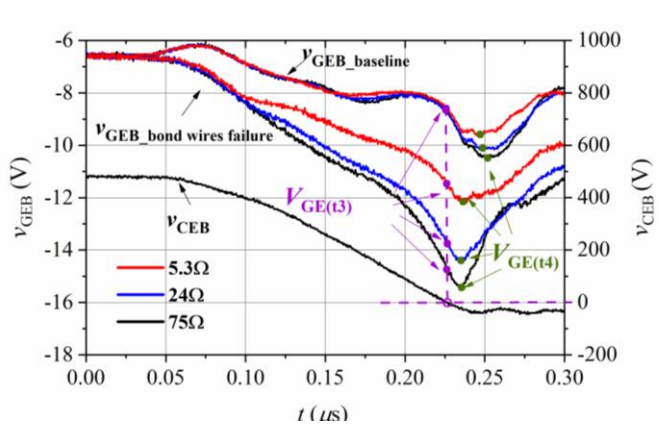
The relative sensitivity (RS) of $V_{GE(t4)}$ and $V_{GE(t3)}$ caused by the bond wires failure can be calculated according to (13):

$$\text{Relative Sensitivity} = \frac{\left|V_{GE\_bond\ wires\ failure}\right| - \left|V_{GE\_baseline}\right|}{\left|V_{GE\_bond\ wires\ failure}\right| - V_{GB}} \times 100\% \quad (13)$$

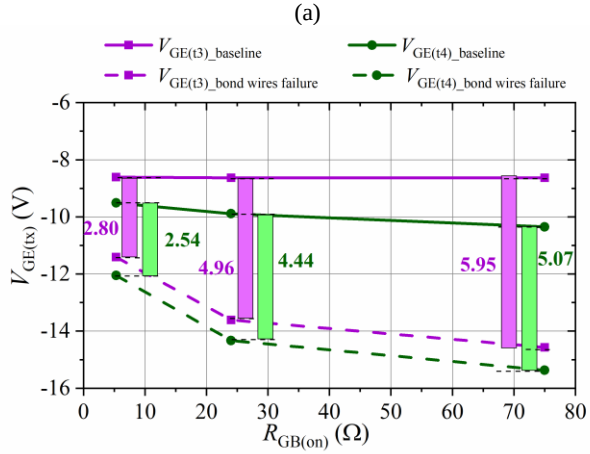
Definition (13) is to make a horizontal comparison of the influence of gate resistance, load current and junction temperature on the monitoring method.

It can be calculated that the RS of $V_{GE(t4)}$ to monitor bond wires failure is 67.67%, which has less relative sensitivity to the bond wires failure comparing with the 73.28% of $V_{GE(t3)}$. The reason is that $V_{GE(t4)}$ is composed of two parts as shown in (12), and $|\Delta V_{GE}|$ in the baseline curve is larger than that in the bond wires failure curve, which reduces the relative change in the monitored signal.

Fig.7(b) shows the experimental results of FF600R17ME4. The capacitor voltage is 800V, the temperature is 25°C, and the load current is changed to 100A. The relative sensitivity of is $V_{GE(t4)}$ is 37.03%. The experimental results further verify that the proposed method is suitable for different types of IGBT modules, and further verify the effectiveness of proposed the method. The following discussion takes TXFF450RMC1 experimental results as an example.



(a)



(b)

Fig.8 (a) v_{GEB} changes with $R_{GB(on)}$ after bond wires failure occurs. (b) Behaviors of $V_{GE(t3)}$ and $V_{GE(t4)}$ with changes with $R_{GB(on)}$ and bond wires failure at 20°C.

A. *The impact of* $R_{GB(on)}$ on monitoring sensitivity

The gate resistance $R_{GB(on)}$ is related to $V_{GE(t3)}$ and $V_{GE(t4)}$ as indicated in (3), therefore, it is necessary to investigate its impact on the monitoring sensitivity. Fig. 8 (a) demonstrates the waveforms of v_{GEB} and v_{CEB} before and after the bond wires failure when $R_{GB(on)}$ is set to 5.3Ω, 24Ω and 75Ω, respectively. Other testing conditions are kept at the capacitor voltage V_{dc} of 500V, the load current I_L of 100A, and the temperature T_j of 20°C. $V_{GE(t3)}$ and $V_{GE(t4)}$ behavior with changes in $R_{GB(on)}$ and bond wires failure is shown Fig.8 (b).

The experimental results show that after $R_{GB(on)}$ is increased, the measured gate voltage waveform of v_{GEB} will reach to a lower negative value, either the IGBT chip is in the state of health or failure. Hence, the monitored parameters of $V_{GE(t3)}$ and $V_{GE(t4)}$ are all impacted when the gate resistor increasing from 5.3Ω to 75 Ω. As compared in Fig. 8 (b), the variation between $V_{GE(t3)\_baseline}$ and $V_{GE(t3)\_\ bond\ wires\ failure}$ increase from 2.80V to 5.95V, while the variation between $V_{GE(t4)\_baseline}$ and $V_{GE(t4)\_\ bond\ wires\ failure}$ increase from 2.54V to 5.07V. Their relative sensitivity to the bond wires failure when applying different $R_{GB(on)}$ is calculated and summarized in TABLE II. It can be seen that with $R_{GB(on)}$ increasing, the relative sensitivity of $V_{GE\ (t3)}$ and $V_{GE(t4)}$ to monitor bond wires failure increases accordingly. $V_{GE(t4)}$-RS is always less than $V_{GE(t3)}$-RS, and the difference between $V_{GE(t4)}$-RS and $V_{GE(t3)}$-RS is less than 15%.

TABLE II
THE RELATIVE SENSITIVITY OF $V_{GE(t3)}$ AND $V_{GE(t4)}$ WITH DIFFERENT $R_{GB(on)}$

$R_{GB(on)}$(Ω)	$V_{GE(t3)}$-RS(%)	$V_{GE(t4)}$-RS(%)
5.3	56.45%	45.36%
24	69.56%	56.35%
75	73.28%	67.67%

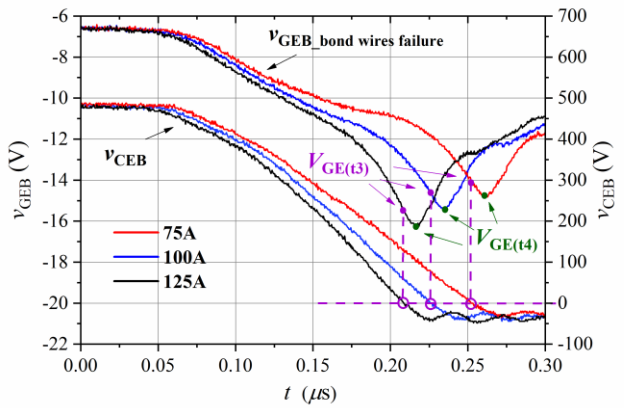
Experimental results show that larger gate resistor can bring greater monitoring sensitivity. During the Q_T turn off process, Changing the gate resistance $R_{GB(on)}$ during the monitoring process does not affect the operating characteristics of the MMC. Therefore, an auxiliary circuit can be added to the drive circuit to appropriately increase $R_{GB(on)}$ during the monitoring process. For IGBT modules with higher rated voltages and higher rated currents, there are more IGBT chips connected in parallel. For example, the IGBT module (DIM800NSM33-F), with 3.3kV rated voltage and 800A rated current, consists of 16 IGBT chips and diodes in parallel. The relative sensitivity of $V_{GE(t3)}$ and $V_{GE(t4)}$ to monitor the bond wires failure among the 16 chips may be small. An auxiliary circuit can be used to appropriately increase the $R_{GB(on)}$ of the monitoring process to obtain sufficient monitoring sensitivity. It should be noted that the gate voltage limit of IGBT devices is usually ±20V. Increasing the gate resistor $R_{GB(on)}$ will increase the negative gate voltage peak, which may damage the gate and cause the risk of device failure. Moreover, the driving circuit should be equipped with a clamping circuit to protect the gate.

B. *Influence of the load current* I_L

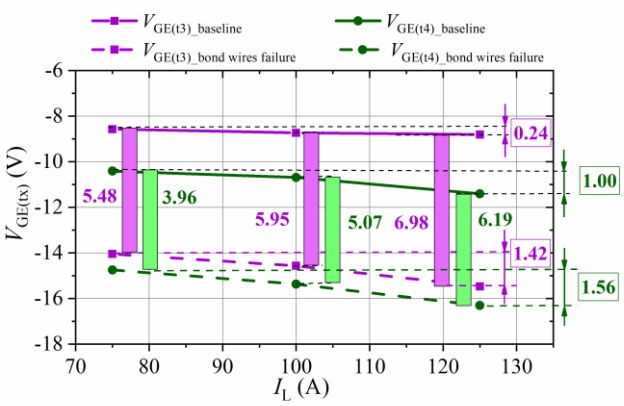
The load current I_L is one of the main factors affecting the accuracy of the failure indicators of $V_{GE(t3)}$ and $V_{GE(t4)}$. Since the load current does not flow through the IGBT Q_B while the diode D_B is reverse-biased during t_2-t_3 stage, the load current I_L only affects the turn-off process of the top IGBT Q_T. Given that dv_{CET}/dt of the controlled IGBT increases with increasing I_L [32], the collector voltage slope k of Q_B increases accordingly. This is because higher I_L requires higher gate voltage at Miller Plateau, which causes larger gate current as a result of increased voltage drop between the gate and the negative drive voltage. This, in turn leads to large displacement current of the Miller capacitance of Q_B and thus the $V_{GE(t3)}$ decrease (negative rise) according to Eq. (3).

During t_3-t_4 stage, the load current I_L affects di_C/dt of the Q_T and thus affects di_{DB}/dt of the D_B. With I_L increasing, the speed of current commutation increases [33], and di_{DB}/dt increases accordingly. Refer to (9) and (10), it can be seen that v_{LS1} increases and $V_{GE(t4)}$ decreases.

The capacitor voltage V_{dc} is 500V, the $R_{GB(on)}$ is 75Ω, and the temperature T_j is 20°C. Fig. 9 (a) demonstrates the waveforms of v_{GEB} after the bond wires failure when I_L is set to 75A, 100A and 125A, respectively. Other testing conditions are kept at the capacitor voltage V_{dc} of 500V, the load current I_L of 100A, and the temperature T_j of 20°C. $V_{GE(t3)}$ and $V_{GE(t4)}$ behavior with changes in I_L and bond wires failure at 20°C is shown in Fig.9 (b). The experimental results show that with I_L increasing, the

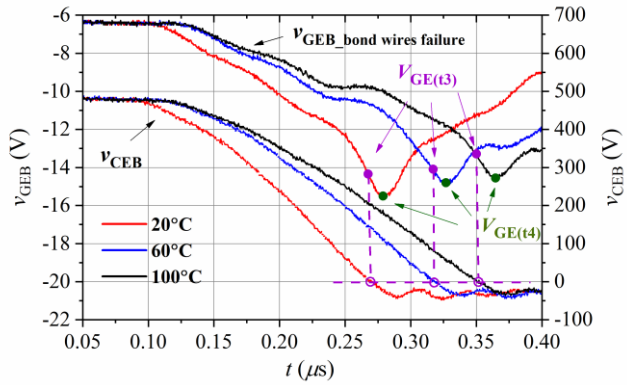


(a)

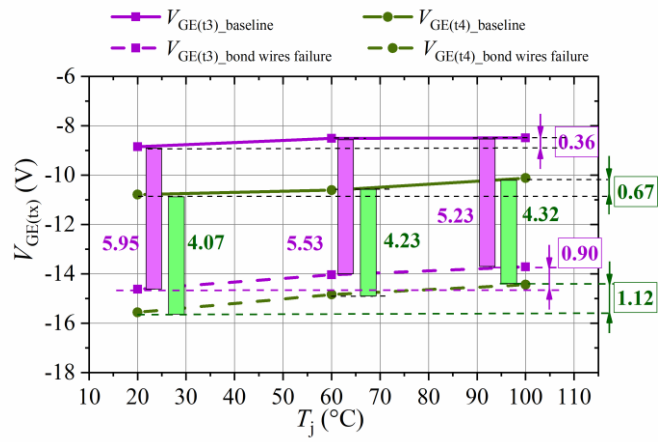


(b)

Fig.9 (a) v_{GEB} changes with I_L after bond wires failure occurs. (b) Behaviors of $V_{GE(t3)}$ and $V_{GE(t4)}$ with changes in I_L and bond wires failure at 20℃.



(a)



(b)

Fig.10 (a) v_{GEB} changes with T_j after bond wires failure occurs. (b) Behaviors of $V_{GE(t3)}$ and $V_{GE(t4)}$ with changes in T_j and bond wires failure at 20℃.

gate voltage v_{GEB} in the baseline state and v_{GEB} with the bond wires failure are all decreased. In the current range of 75A to 125A, $V_{GE(t3)\_baseline}$ is decreased by 0.24V, $V_{GE(t4)\_baseline}$ is decreased by 1.00V.After the bond wires failure, in the current range of 75A to 125A, $V_{GE(t3)\_bond\ wires\ failure}$ decreases by 1.42V. $V_{GE(t4)\_bond\ wires\ failure}$ decreases by 1.56V. Due to the combined effect of the two stages, $V_{GE(t4)}$ is more affected by changes in load current I_L than $V_{GE(t3)}$.

With the load current I_L increasing, the variation between $V_{GE\_baseline}$ and $V_{GE\_bond\ wires\ failure}$ increases and the relative sensitivity also increases. Considering the full loading range in MMC applications, the load current I_L varies following the sinusoidal load, from zero current to the rated current 450A. With such a large variation, the influence of I_L on $V_{GE(t3)}$ and $V_{GE(t4)}$ cannot be ignored. Therefore, the statistical approach to improved accuracy is proposed in the next section, which leverage the mean value and RMS value of the failure indicators.

C. Influence of the junction temperature T_j

The influence of temperature T_j can be divided into two parts: 1) affect the turn-off process of the top IGBT Q_T. With the temperature T_j increasing, dv_{CET}/dt of Q_T decreases [32], and the collector voltage change rate k of Q_B decreases accordingly. Refer to (3), it can be seen that $V_{GE(t3)}$ increases. With the temperature T_j increasing, $-di_C/dt$ decreases [33]and di_{DB}/dt decreases accordingly. Refer to (9) and (10), it can be seen that v_{LS1} decreases and $V_{GE(t4)}$ increases. 2) affect the temperature sensitive parameters of the bottom IGBT Q_B, such as the Miller capacitor C_{GCB} [34]and gate resistance, etc.

The temperature controlled by the heat plate is set to 20℃, 60℃, and 100℃. The temperature of the IGBT module is measured from embedded NTC temperature sensor. During the experiment, the capacitor voltage V_{dc} is 500V, the load current I_L is 100A, and the gate resistance $R_{GB(on)}$ is 75Ω. Fig. 10 (a) demonstrates the waveforms of v_{GEB} after the bond wires failure with changes in T_j. $V_{GE(t3)}$ and $V_{GE(t4)}$ behavior with changes in T_j and IGBT bond wires failure is shown in Fig.10 (b).

The experimental results show that I_L increases, the v_{GEB} in the baseline state and v_{GEB} with bond wires failure are all increased. In the temperature range of 20℃ to 100℃, $V_{GE(t3)\_baseline}$ increases by 0.36V. Due to the superposition of the two stages, $V_{GE(t4)\_baseline}$ is decreased by 0.67V. After the bond wires failure, in the temperature range of 20℃ to 100℃, $V_{GE(t3)\_bond\ wires\ failure}$ increased by 0.90V. $V_{GE(t4)\_bond\ wires\ failure}$ increased by 1.12V. $V_{GE(t4)}$ is more affected by changes in temperature T_j than $V_{GE(t3)}$.

As the T_j increases, the variation between $V_{GE\_baseline}$ and $V_{GE\_bond\ wires\ failure}$ decreases and the relative sensitivity also decreases. The variation between $V_{GE(t4)\_baseline}$ at 20℃ and $V_{GE(t4)\_bond\ wires\ failure}$ at 100℃ is 3.65V, which is the minimum variation in the range of 20℃ to 100℃. This minimum variation is used as the numerator of (13). $V_{GE(t4)\_bond\ wires\ failure}$ at 20℃ is used as the

denominator of (13), which is the maximum value in the range of 20°C to 100°C. Therefor the minimum relative sensitivity of $V_{GE(t4)}$ calculated is 40.07%. Similarly, the minimum relative sensitivity of $V_{GE(t3)}$ calculated is 59.61%.

The gate resistor $R_{GB(on)}$ is replaced with 5.3Ω and the experiment of changing temperature T_j with IGBT failure is repeated. The minimum relative sensitivity of $V_{GE(t4)}$ in the range of 20°C to 100°C is 39.98%. Therefore, the temperature fluctuation can be ignored during the field operation under maximum allowable temperature.

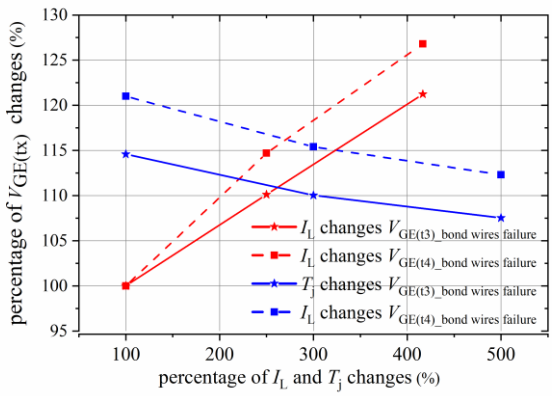


Fig.11 Percentage of $V_{GE(tx)\_bond\ wires\ falure}$ changes with I_L and T_j

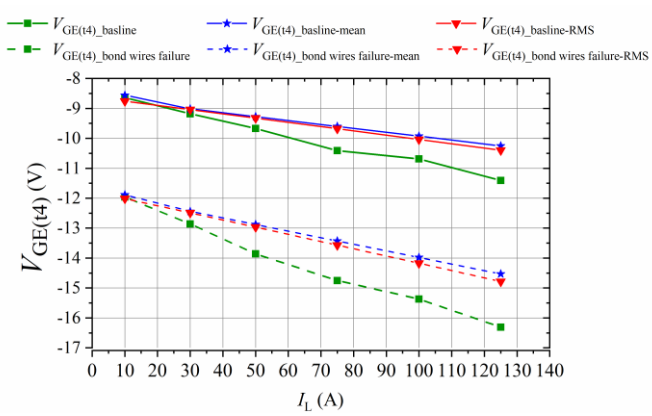


Fig.12 Relationship between $V_{GE(t4)}$ and I_L

IV. Comparison of $V_{GE(T3)}$ and $V_{GE(T4)}$

Based on the experimental results, the $V_{GE(tx)\_bond\ wires\ failure}$ with the load current of 30A at 20°C is taken as the reference value. 30A is taken as the reference value of load current, and 20°C is taken as the reference value of temperature. The percentage of $V_{GE(t4)}$ changes with I_L and T_j is shown as Fig.11. Compared to the temperature, the load current has more influence on $V_{GE(t3)\_bond\ wires\ failure}$ and $V_{GE(t4)\_bond\ wires\ failure}$.

In the MMC application, since the load current I_L changes with the current on the AC side of the MMC, the current fluctuates from 0 to the MMC rated current range, and its influence on $V_{GE(t3)}$ and $V_{GE(t4)}$ cannot be ignored. In the temperature range of 20°C to 100°C, the minimum relative sensitivity of $V_{GE(t3)}$ and $V_{GE(t4)}$ are acceptable, hence there is no need to monitor the junction temperature. Compared with $V_{GE(t4)}$, $V_{GE(t3)}$ is less affected by load current and temperature, and has the higher relative sensitivity. It is worth noting that the relative sensitivity of $V_{GE(t4)}$ with the bond wires failure is more than 40%, as shown in TABLE II, which can also meet the monitoring requirements.

For the monitoring device implementation, $V_{GE(t3)}$ is the gate voltage at t_3, which is realized by measuring the gate voltage when the collector voltage is zero. Additional voltage measurement points and signal processing circuits need to be added. The collector voltage measurement also needs to isolate the high voltage. Furthermore, in the transient process of the turn-off process, $V_{GE(t3)}$ accurate measurement puts forward higher requirements on the time delay of the signal processing circuit. In contrast to that, $V_{GE\ (t4)}$ does not require additional voltage measurement points, and peak measurement is easy to implement. Based on the above analysis, it can be seen that the $V_{GE(t4)}$ is more suitable as an online monitoring feature quantity for bond wires failure in the MMC submodules.

When $V_{GE(t4)}$ is used as the feature quantity to monitor bond wires failure in MMC, the threshold of failure criterion needs to be adjusted according to the load current. There are two threshold setting modes:

1) *Mode 1*: the instantaneous $V_{GE(t4)}$ of separate turn-off process is used to monitor bond wires failure in MMC. The relationship between $V_{GE(t4)}$ and instantaneous shutdown current I_L corresponds to the green lines in Fig.12. $V_{GE(t4)\_baseline}$ and $V_{GE(t4)\_bond\ wires\ failure}$ decrease with increasing I_L in an approximately linear manner. The following relationship can be obtained by fitting the experimental data:

$$V_{GE(t4)\_baseline}(I_L) = -0.022 I_L - 8.62 \tag{14}$$

$$V_{GE(t4)\_bond\ wires\ failure}(I_L) = -0.037 I_L - 11.78 \tag{15}$$

Equation (15) can be used as a reference for $V_{GE(t4)}$ to monitor the bond wires failure threshold criterion as the instantaneous shutdown current changes.

2) *Mode 2*: the mean value and RMS value of $V_{GE(t4)}$ in a fundamental period of AC current is used to monitor bond wires failure. The AC fundamental frequency of MMC is f_0, and the switching frequency of IGBT module in SMs is f_s. Despite many modulation techniques including third-harmonic PWM, space vector modulation, etc., the most basic sinusoidal PWM technique is assumed for simplicity, where the PWM falling edge-aligned to control. By neglecting the deadtime, the mean value for the positive half cycle of load current can be measured to improve accuracy. Their baseline curves are derived from that for instantaneous values.

The total number N of IGBT Q_T turning-offs in a fundamental period is:

$$N = \frac{f_s}{2 f_0} \tag{16}$$

The instantaneous current I_{Ln} at the nth turn-off of Q_T in the fundamental period is

$$I_{Ln} = I_L \sin\left(\frac{2 f_0 \pi}{f_s} n\right) \quad (n = 1, 2, \cdots N) \tag{17}$$

Combined the (14), (15), (17), the mean value of $V_{GE(t4)}$ is:

$$V_{\mathrm{GE(t4)-mean}} = \sum_{n=1}^{N} V_{\mathrm{GE(t4)}}\left(I_{\mathrm{Ln}}\right) \Big/ N \tag{18}$$

The calculation result of $V_{\mathrm{GE(t4)\_baseline\text{-}mean}}$ and $V_{\mathrm{GE(t4)\_bond\ wires\ failure\text{-}mean}}$ is shown in the Fig.12 by the blue line, and $V_{\mathrm{GE(t4)\_baseline}}$-mean and $V_{\mathrm{GE(t4)\_bond\ wires\ failure\text{-}mean}}$ decreases with AC peak current I_{L} in an approximately linear manner. The following relationship can be obtained by fitting the data:

$$V_{\mathrm{GE(t4)\_baseline-mean}}\left(I_{\mathrm{L}}\right) = -0.014 I_{\mathrm{L}} - 8.62 \tag{19}$$

$$V_{\mathrm{GE(t4)\_bond\ wires\ failure-mean}}\left(I_{\mathrm{L}}\right) = -0.023 I_{\mathrm{L}} - 11.78 \tag{20}$$

The RMS value of $V_{\mathrm{GE(t4)}}$ is:

$$V_{\mathrm{GE(t4)-RMS}} = -\sqrt{\sum_{n=1}^{N} V_{\mathrm{GE(t4)}}^{2}\left(I_{\mathrm{Ln}}\right) \Big/ N} \tag{21}$$

The calculation result of $V_{\mathrm{GE(t4)\_baseline\text{-}RMS}}$ and $V_{\mathrm{GE(t4)\_bond\ wires\ failure\text{-}RMS}}$ is shown in the Fig.12 by the red line, and $V_{\mathrm{GE(t4)\_baseline\text{-}RMS}}$ and $V_{\mathrm{GE(t4)\_bond\ wires\ failure\text{-}RMS}}$ decreases with AC peak current I_{L} in an approximately linear manner. The relationship between $V_{\mathrm{GE(t4)\text{-}mean}}$ and $V_{\mathrm{GE(t4)\text{-}RMS}}$ changes with AC peak current I_{L} is basically the same.

The $V_{\mathrm{GE(t4)\text{-}mean}}$ and $V_{\mathrm{GE(t4)\text{-}RMS}}$ can eliminate the interference of measurement noise to improve the accuracy of monitoring, and the change of $V_{\mathrm{GE(t4)\text{-}mean}}$ with $V_{\mathrm{GE(t4)\text{-}RMS}}$ has better linearity. Under the premise of meeting the monitoring sensitivity, *Mode 2* is more suitable for online monitoring.

V. Measurement Implementation Discussion

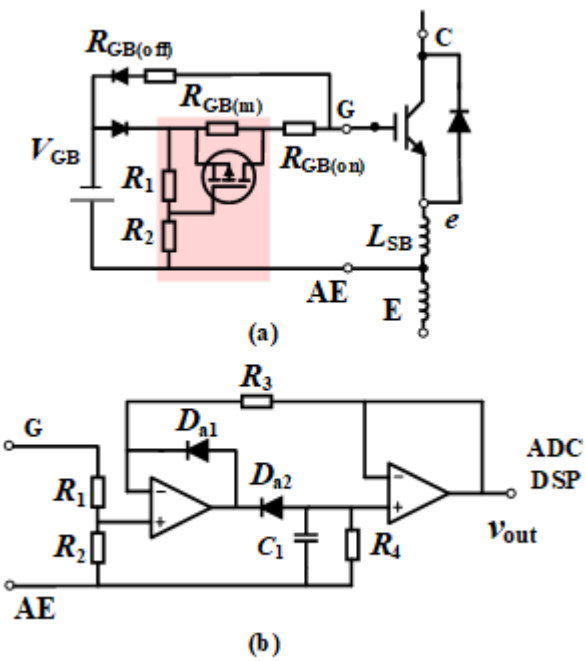


Fig.13 (a) Schematic of increasing the gate resistance during monitoring. (b) Schematic of the $V_{\mathrm{GE(t4)}}$ measurement circuit

After establishing the above failure indicators, their feasibility for in-situ measurement will be discussed using Fig. 13. Fig.13(a) shows the schematic of the gate resistance selection circuit. The main function of this circuit is to temporarily increase the gate resistance during the health monitoring process without changing the gate resistance during the normal switching transition. During the normal IGBT turn-off transient, the driving power supply voltage is negative with reference to the terminal AE, and the driving current flows through the $R_{\mathrm{GB(off)}}$ branch. When the IGBT is turned on for the normal switching condition, the driving power supply is positive to drive the gate current flowing through the $R_{\mathrm{GB(on)}}$ branch. Since, at this time, the p-channel MOS in the red frame is turned on, $R_{\mathrm{GB(m)}}$ is bypassed and the resultant gate resistance is $R_{\mathrm{GB(on)}}$. Under the monitoring mode, the monitored IGBT switch is in the off state driven by a negative gate voltage, while the complementary controlled IGBT is switched off. According to the above theoretical analysis, the Miller capacitance of the monitored IGBT switch will be discharged due to the crosstalk effect, sinking the gate current through the $R_{\mathrm{GB(on)}}$ branch. At this time, the gate voltage is negative, the p-channel MOS is turned off, and the resultant gate resistance is $R_{\mathrm{GB(on)}}$+$R_{\mathrm{GB(m)}}$. Fig.13(b) shows the schematic of the analog front-end circuit for the $V_{\mathrm{GE(t4)}}$ measurement, which detect and capture the gate voltage peak value, that is the undershoot $V_{\mathrm{GE(t4)}}$. Subsequently, this $V_{\mathrm{GE(t4)}}$ value can be obtained using an analog-to-digital converters (ADC) for post-processing.

VI. Conclusion

This paper has demonstrated a condition monitoring method dedicated to typical bond wires-induced chip open appearing in multichip IGBT submodules in an MMC application. Dedicated failure indicators based on the switching (dynamic) characteristics in a typical hard-switching half-bridge configuration are herein proposed for condition monitoring. The gate voltage of the complementary IGBT switch is measured and by leveraging the crosstalk phenomenon occurring in the turn-off switching transition, its deviation from baseline is related to the health status of its bond wires. Two specific values are selected as failure indicators for monitoring due to their pronounced time stamps: 1) the gate voltage $V_{\mathrm{GE(t3)}}$ at the time when the collector voltage is zero, and 2) the undershoot of the gate voltage $V_{\mathrm{GE(t4)}}$ when the complementary controlled switch in the turn-off switching transition. Through experiments, the sensitivity and stability of both failure indicators were compared.

The main conclusions are as follows:

1) $V_{\mathrm{GE(t3)}}$ is more sensitive than $V_{\mathrm{GE(t4)}}$ in monitoring chip open induced by bond wire lift-off, while being comparably less dependent on the load current and junctional temperature with respect to $V_{\mathrm{GE(t4)}}$.

2) The influence of the junction temperature is negligibly small for both failure indicator, however, the impact of load current variation needs to be taken into account, which manifest itself in a linear function.

3) Compared with instantaneous value of $V_{\mathrm{GE(t4)}}$, the mean value and RMS value of $V_{\mathrm{GE(t4)}}$ obtained by using the half-cycle load current has higher measurement accuracy and linearity, which are suitable for online monitoring.

4) Additional zero-triggering or undershoot-triggering functions is required for measuring $V_{\mathrm{GE(t3)}}$ and $V_{\mathrm{GE(t4)}}$, respectively, for in-circuit measurement, which demand the adjudication of complex gate drivers.

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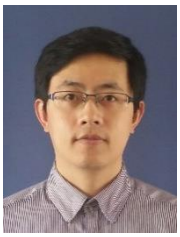

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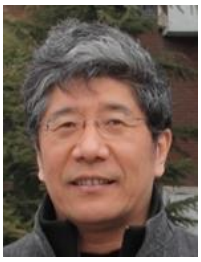

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